# 1. LTPS-TFT研發潮流

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*Thin-film Devices Labo.*

# 課程內容

## 1. 前言

創新

## 2. 薄膜電晶體與顯示器

薄膜電晶體與顯示器

MOS電晶體元件物理

## 3. 次世代LTPS-TFT之研發

矽膜之雷射退火結晶化技術介紹

結晶粒徑增大技術

橫向長晶技術

次世代絕緣膜技術

## 4. 對學生之期許

## 1. 前言

什麼是創新?

創新 ≠ 前瞻≠搞怪

推翻常識的”No.1”

ex. 讓燈絲發光的愛迪生
提出專業晶圓代工產業模式的張忠謀
以GaN作出LED的Nakamura
確立獨自音樂風格的周杰倫
鼎泰豐

各行各業, 無論前瞻與否
創新 → 創造大產值

要能不受縛於常識, 要能反向思考

什麼是非創新?

後知後覺. 模仿.

無法創造新產值, 所以總在思考如何降成本

ex. 國內面板廠(友達, 奇美, 華映…),

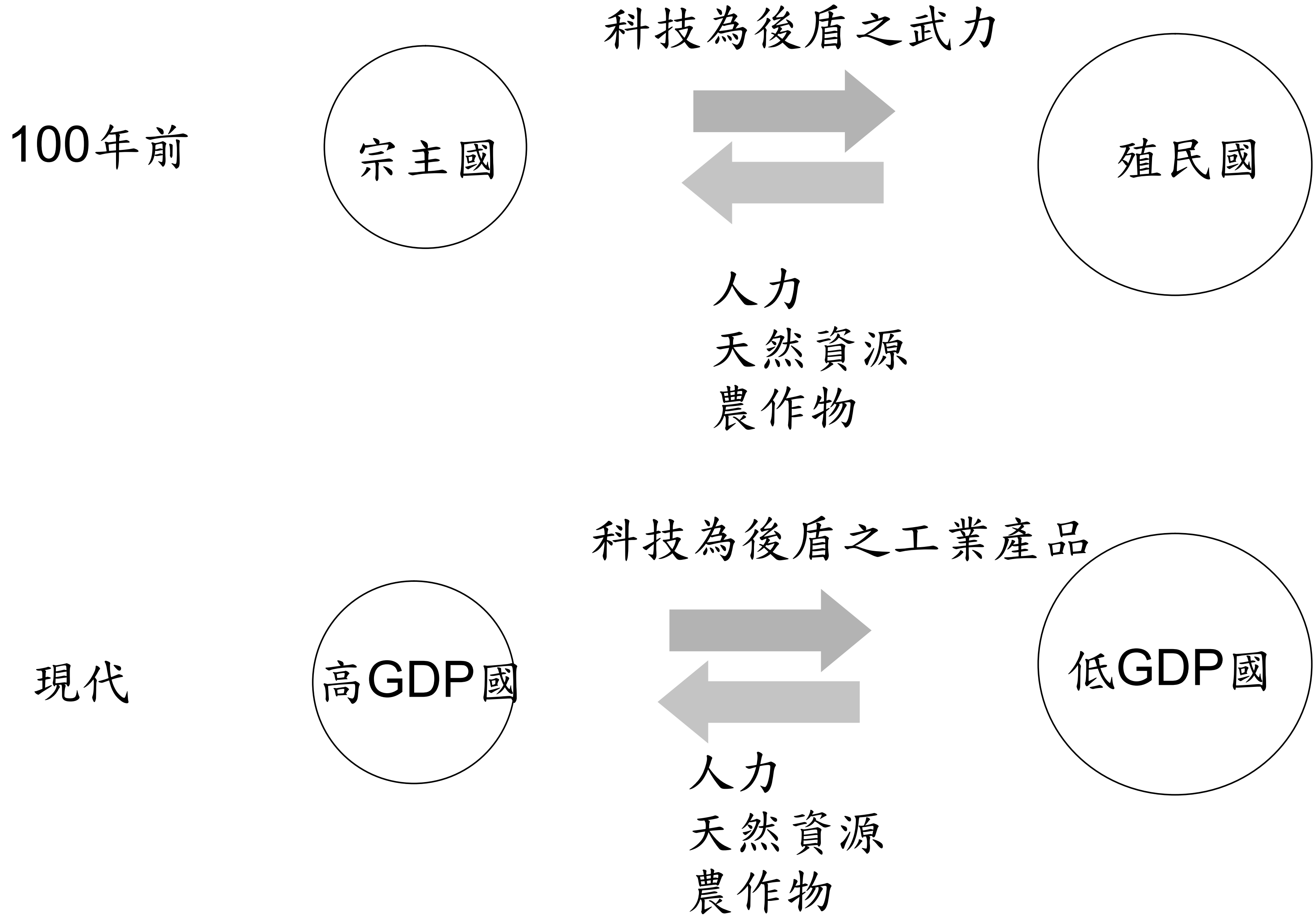
所謂的研發總是” 開發日韓廠已開發完成的技術”

某面板廠副總的話: 『期待學術界幫我們降低成本』

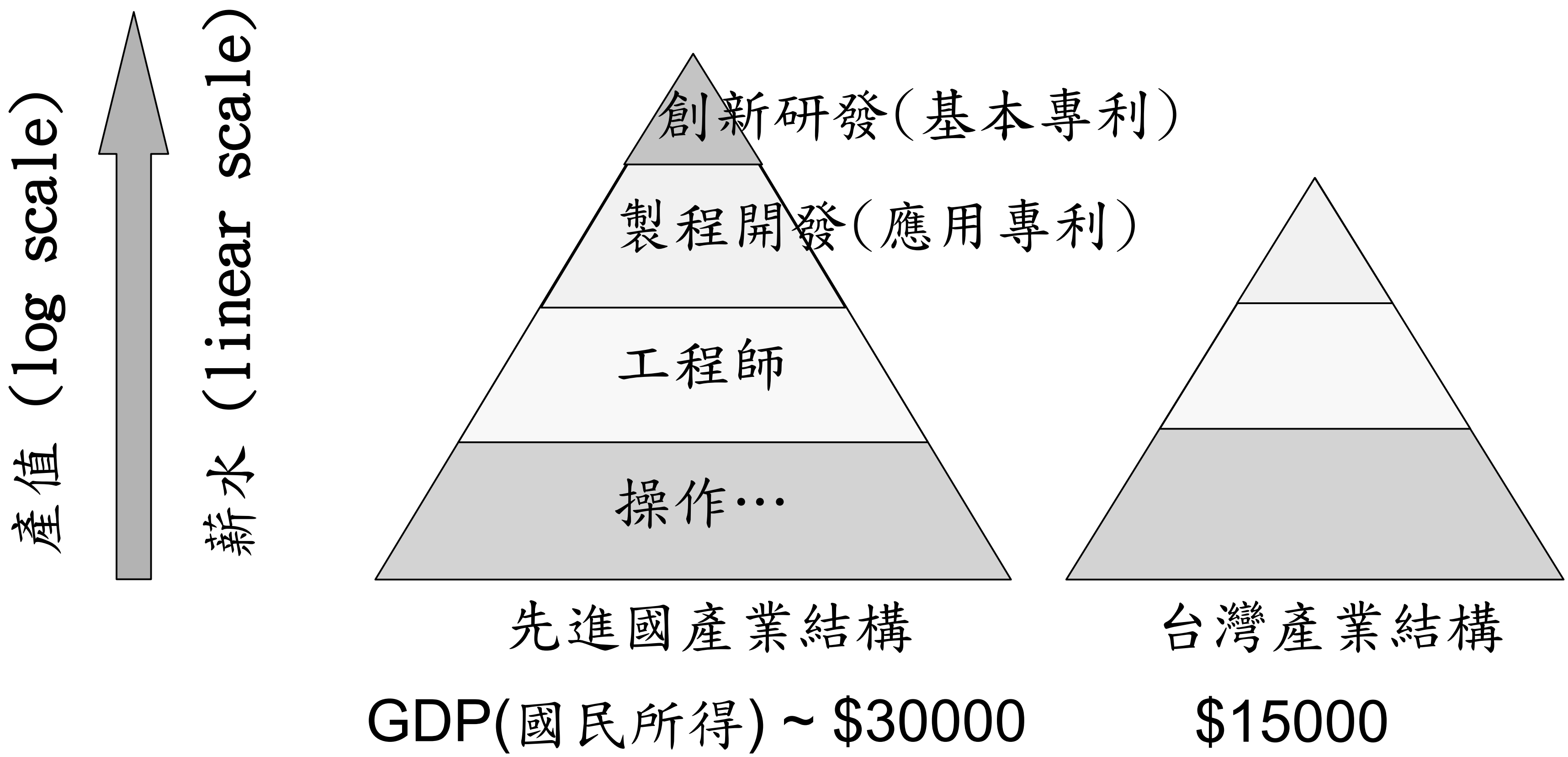
為使經濟更上一層樓, 國民思維需要大轉變,

不能只會模仿代工(友達,奇美, 華映…, )

否則中國也會模仿, 則在未來兩極化的世界競爭中落入被殖民群中


100年前
宗主國
科技為後盾之武力
殖民國
人力
天然資源
農作物
現代
高GDP國
科技為後盾之工業產品
低GDP國
人力
天然資源
農作物

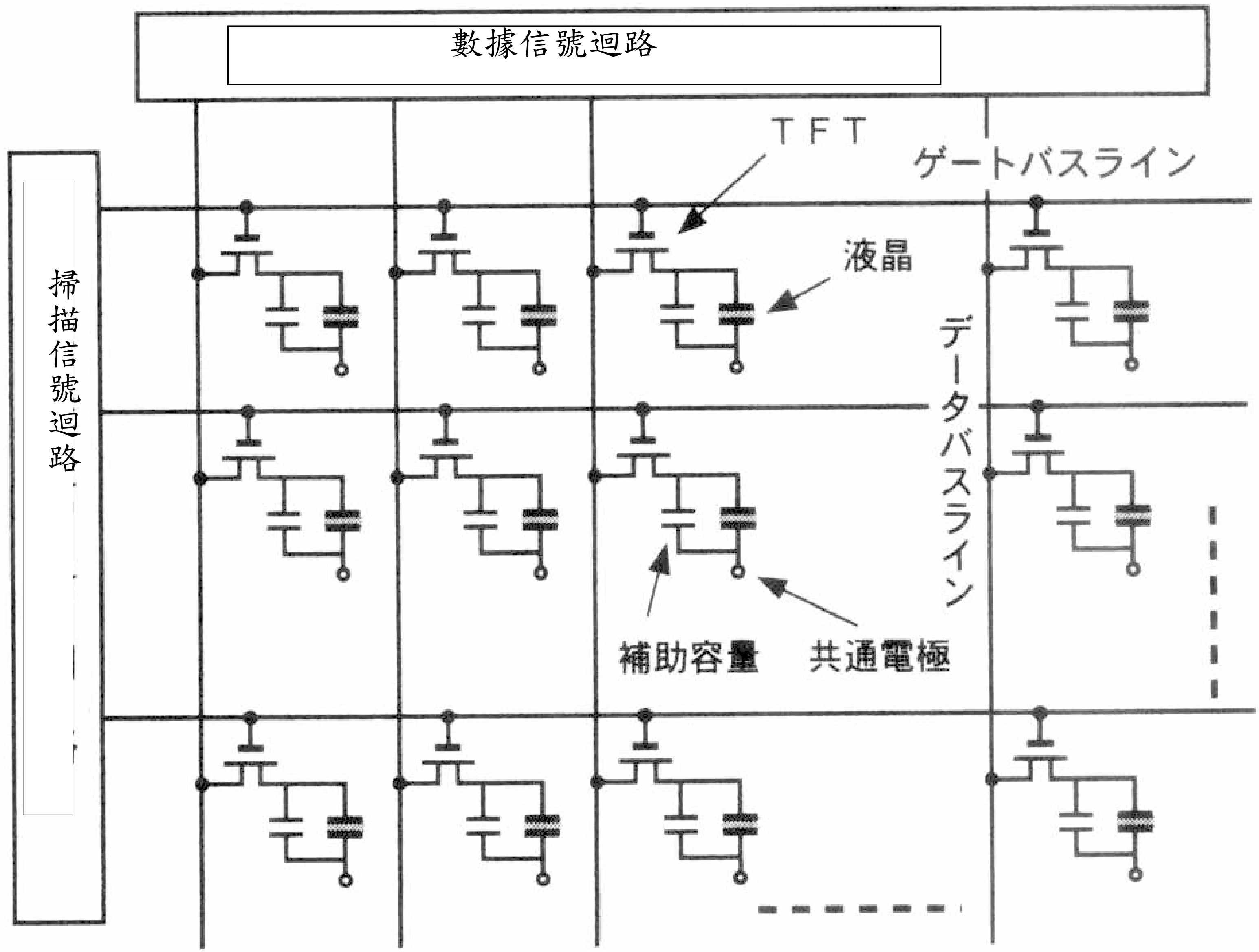
日美歐與台灣產業型態之比較



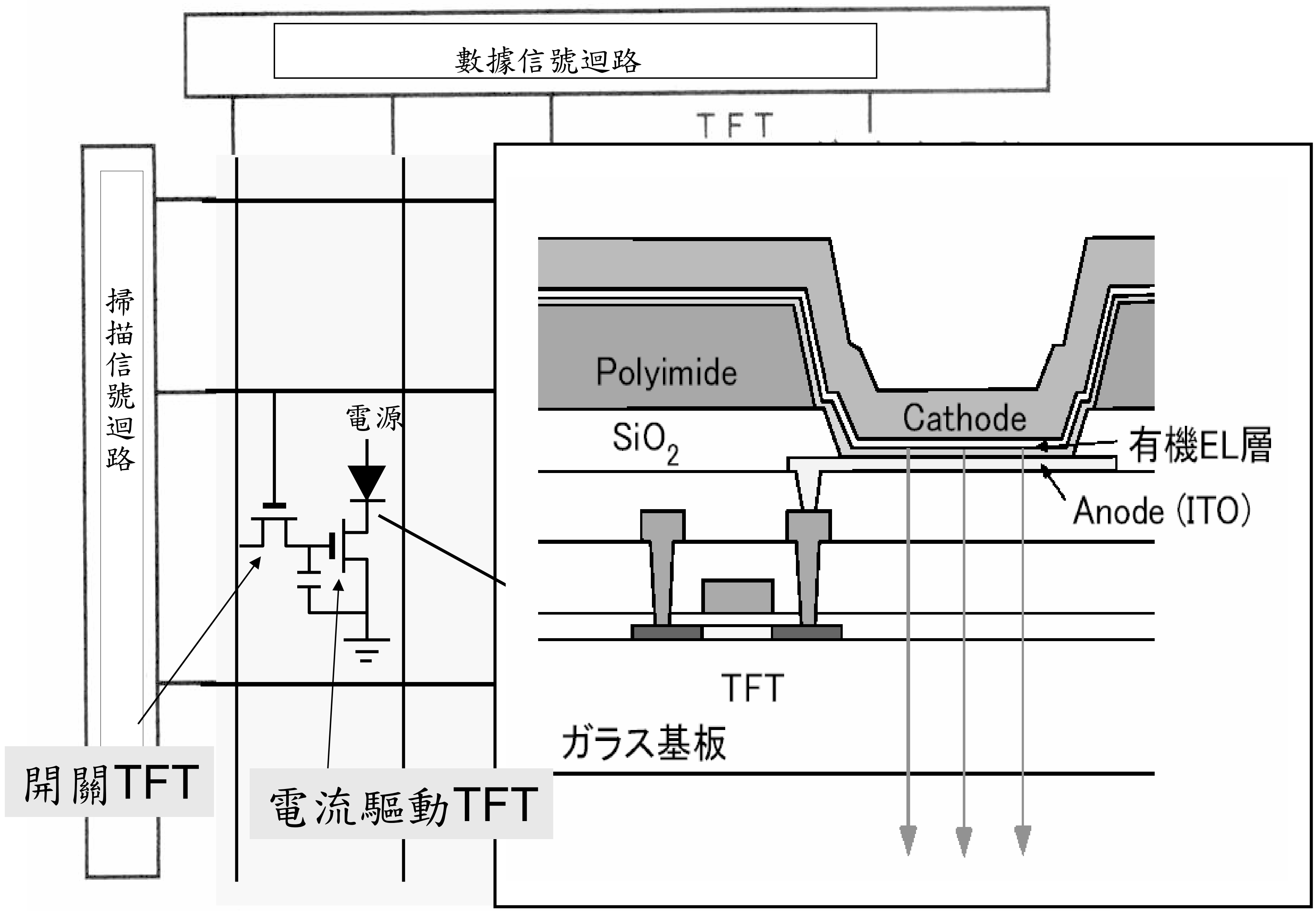
# 2. 薄膜電晶體與顯示器

TFT在面板上之應用

1. 作為畫素開關
2. 畫素之電流驅動電晶體 (電流驅動型畫素)
3. 替代周邊驅動IC
4. 替代LSI, 形成System on panel(SOP)

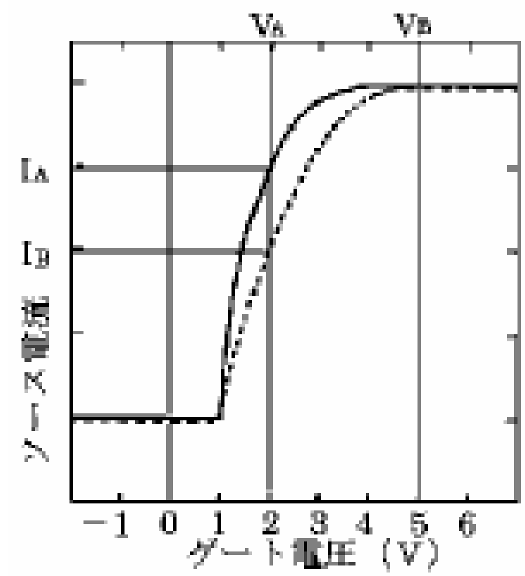

數據信號迴路
TFT
ゲートバスライン
掃描信號迴路
液晶
データバスライン
補助容量
共通電極

以TFT形成週邊驅動電路之液晶顯示器(左)
與傳統市驅動電路外接顯示器之比較



數據信號迴路
TFT
掃描信號迴路
電源
Polyimide
Cathode
SiO2
有機EL層
Anode (ITO)
TFT
ガラス基板
開關TFT
電流驅動TFT

☆ ΔVth造成電流差異 →



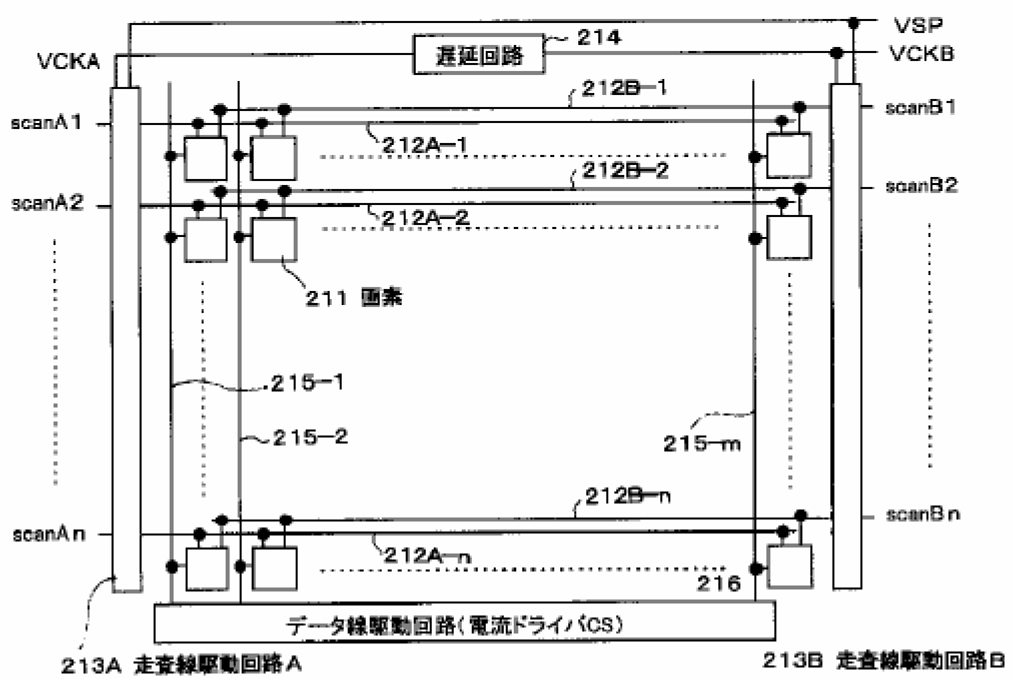

解決方法:

1. 使用不易受ΔVth影響之驅動回路
2. 製造具有極高均一電性之TFT --- 後章節

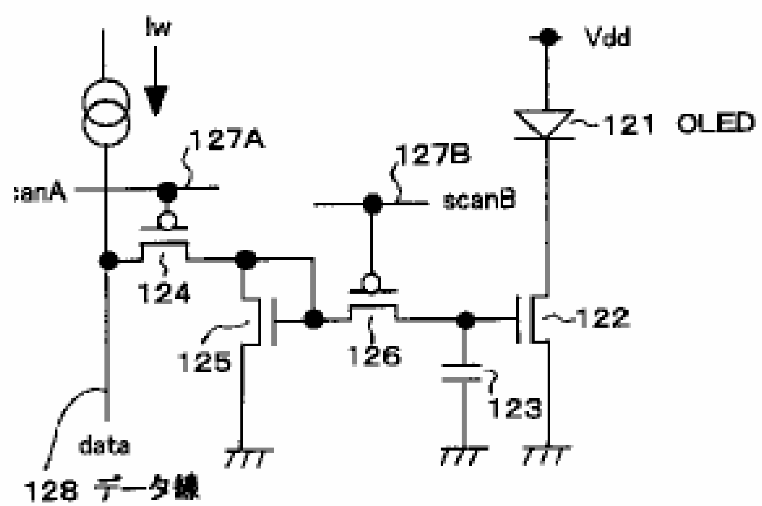
# 2.電流寫入類比控制(1)　(Sony, 2002公開)

## 利用Current mirror回路

【図１６】




【図１４】



TFT125 : 飽和區動作(Vds>Vgs-Vth)

$$I_w = \mu_1 C_{ox1} W_1/2L_1 \ * (V_{gs}-V_{th1})^2$$

TFT122 : 一般為飽和區動作

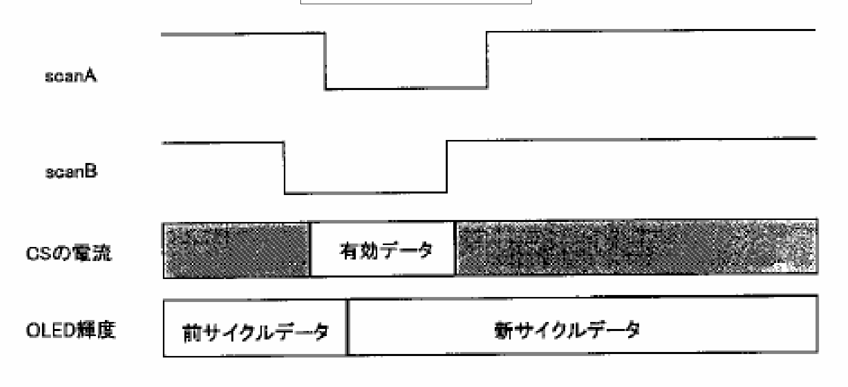
$$I_{drv} = \mu_2 C_{ox2} W_2/2L_2 \ * (V_{gs}-V_{th2})^2$$

由於兩TFT在同一畫素區域中,
因此可視Vth1=Vth2, Cox1=Cox2, μ1= μ2

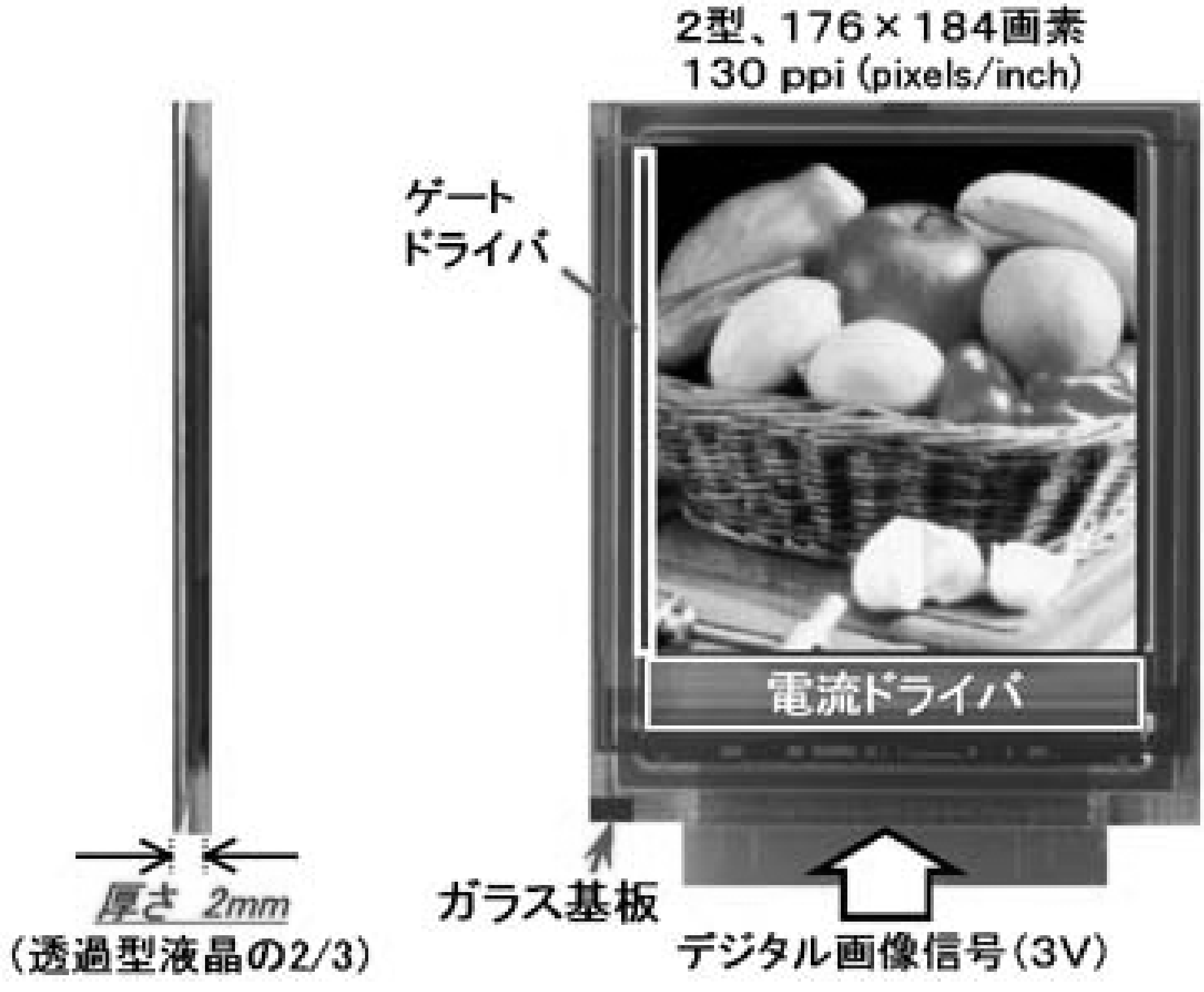
$$\Rightarrow \quad I_{drv}/I_w = (W_2/W_1)/(L_2/L_1)$$

$$\boldsymbol{I_{drv} \ \alpha \ I_w}$$

Timing

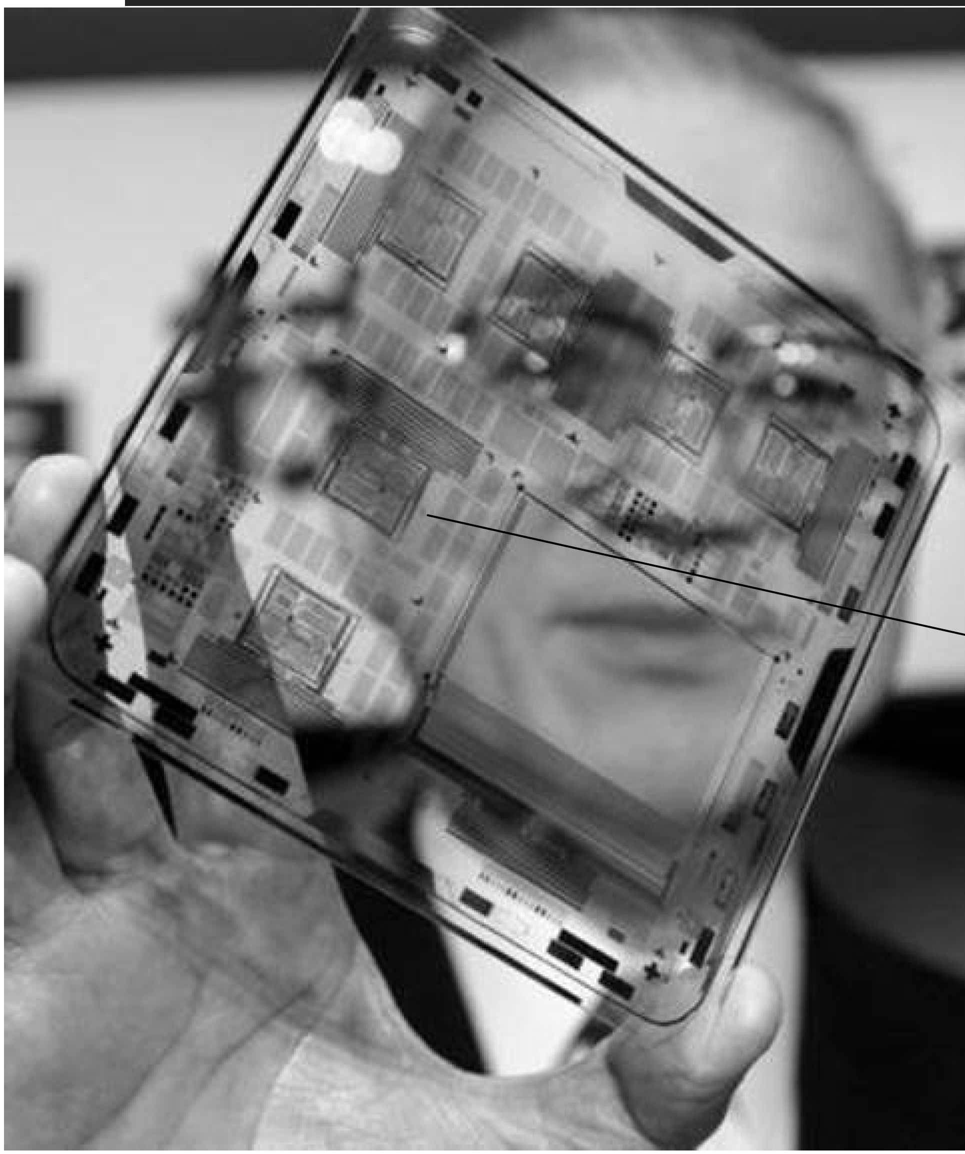


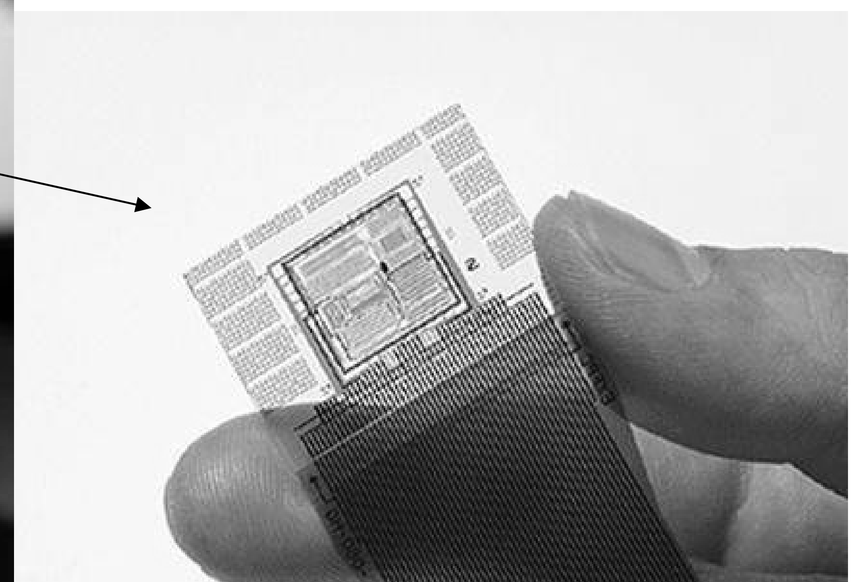
以TFT形成週邊驅動電路之OLED顯示器 (NEC)



# 以TFT製作CPU, 及Memory之嘗試

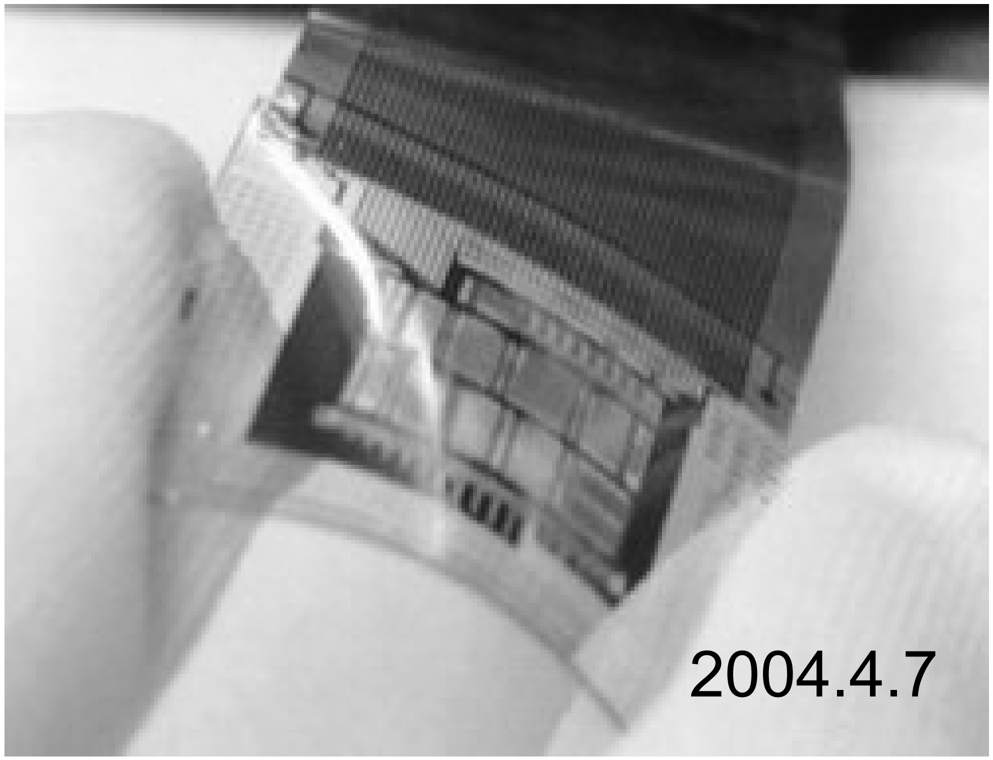
## LTPS-TFT 3MHz Z-80 CPU by Sharp, 2003.3





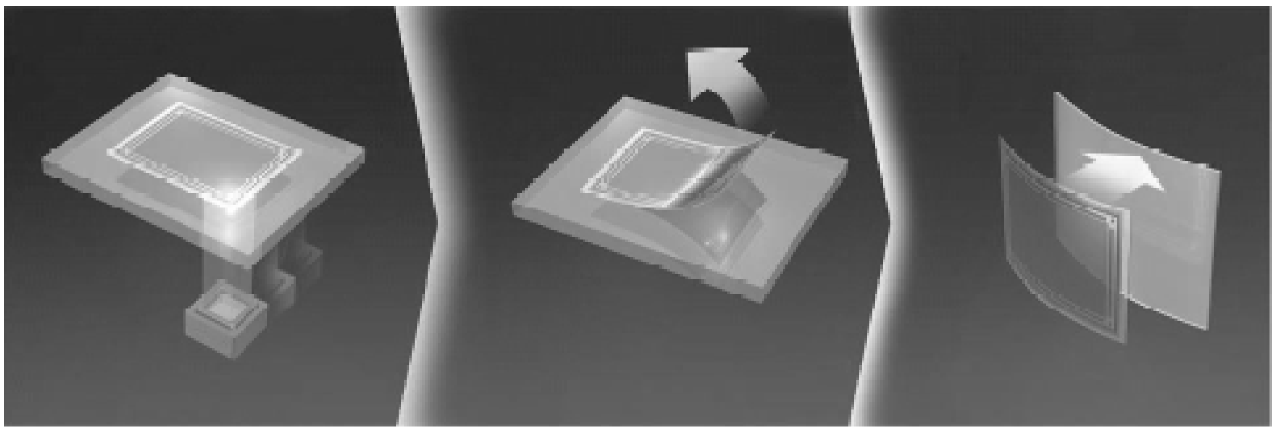
ガラス基板上に形成したCPU<Z80>

# 以玻璃TFT-CPU啟動舊電腦



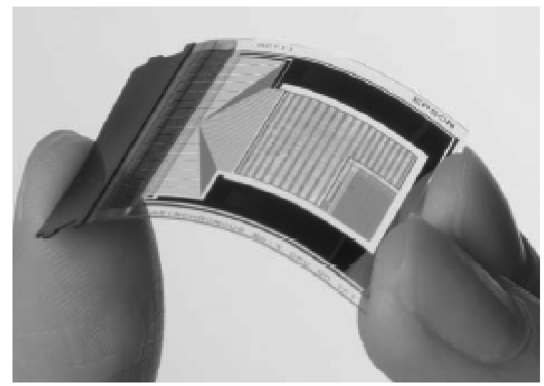

SEL之Z80 CPU by TFT on plastic

# SEIKO EPSON所製作在塑膠上TFT所形成之非同步CPU

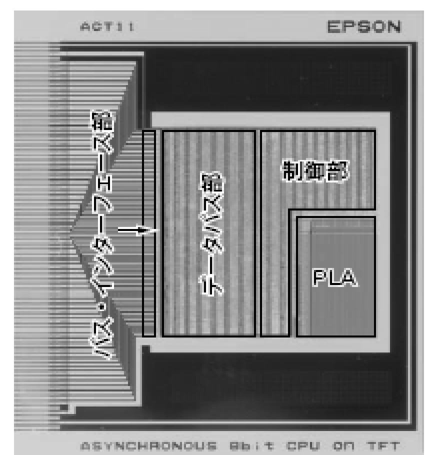


(a) レーザ光の照射　(b) TFT層のはく離　(c) プラスチック基板への転写

図2　SUFTLAフレキシブル実装技術 [3]



(a) フレキシブル8ビット非同期プロセッサ




(b) チップの拡大写真

**写真1**
**今回試作した非同期プロセッサ**
**「ACT11」**

(a)のように柔軟に曲げることができる. CPUコア部の外形寸法は12.5mm角. 約32,000個のTFTトランジスタによって形成されている. 500kHzのサイクル・レートで動作させたときの消費電流は約180 $\mu$A. (b)のPLA (programmable logic array)には約3.5Kバイト相当のマイクロ・コードを格納している. PLAのほか, データバス部, 制御部, バス・インターフェース部から構成されている.

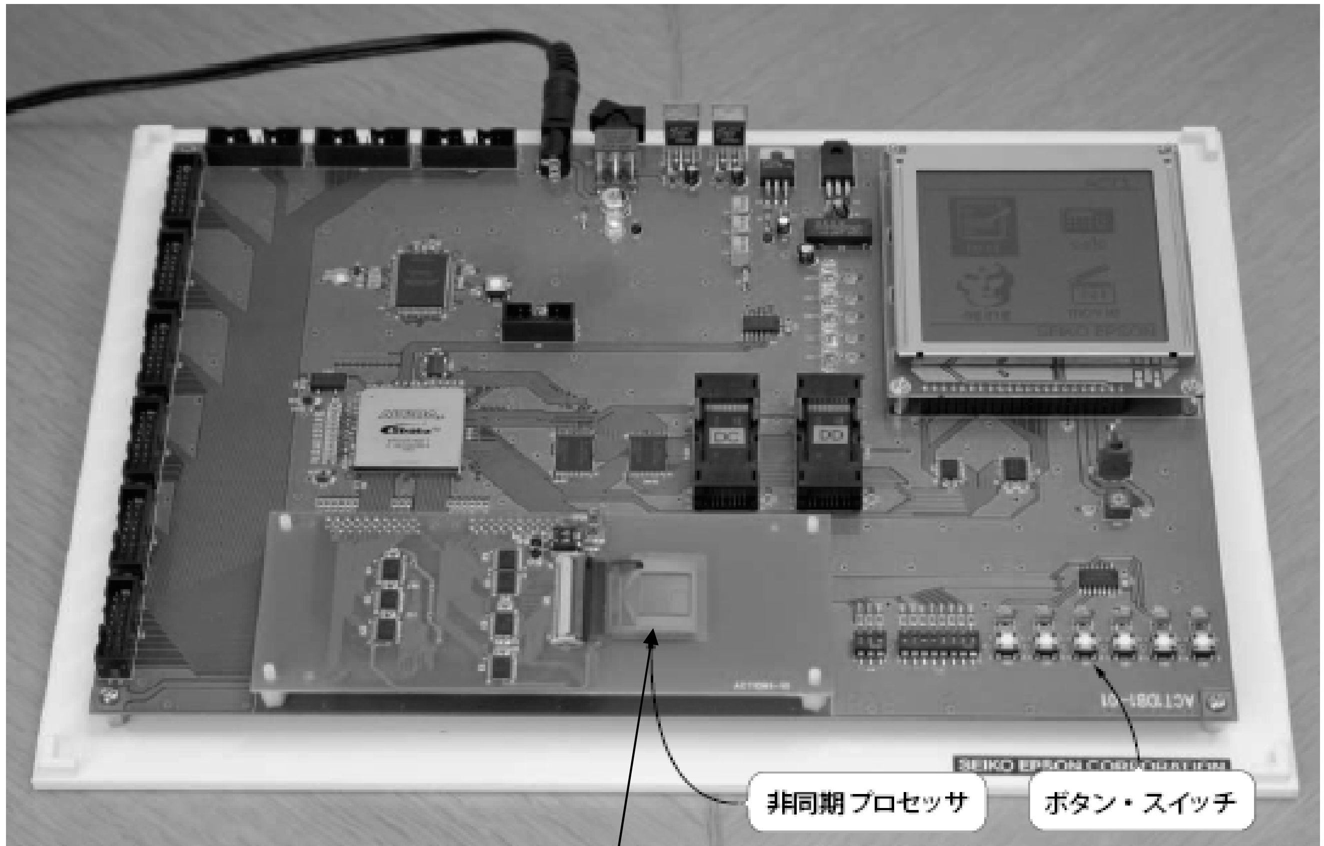
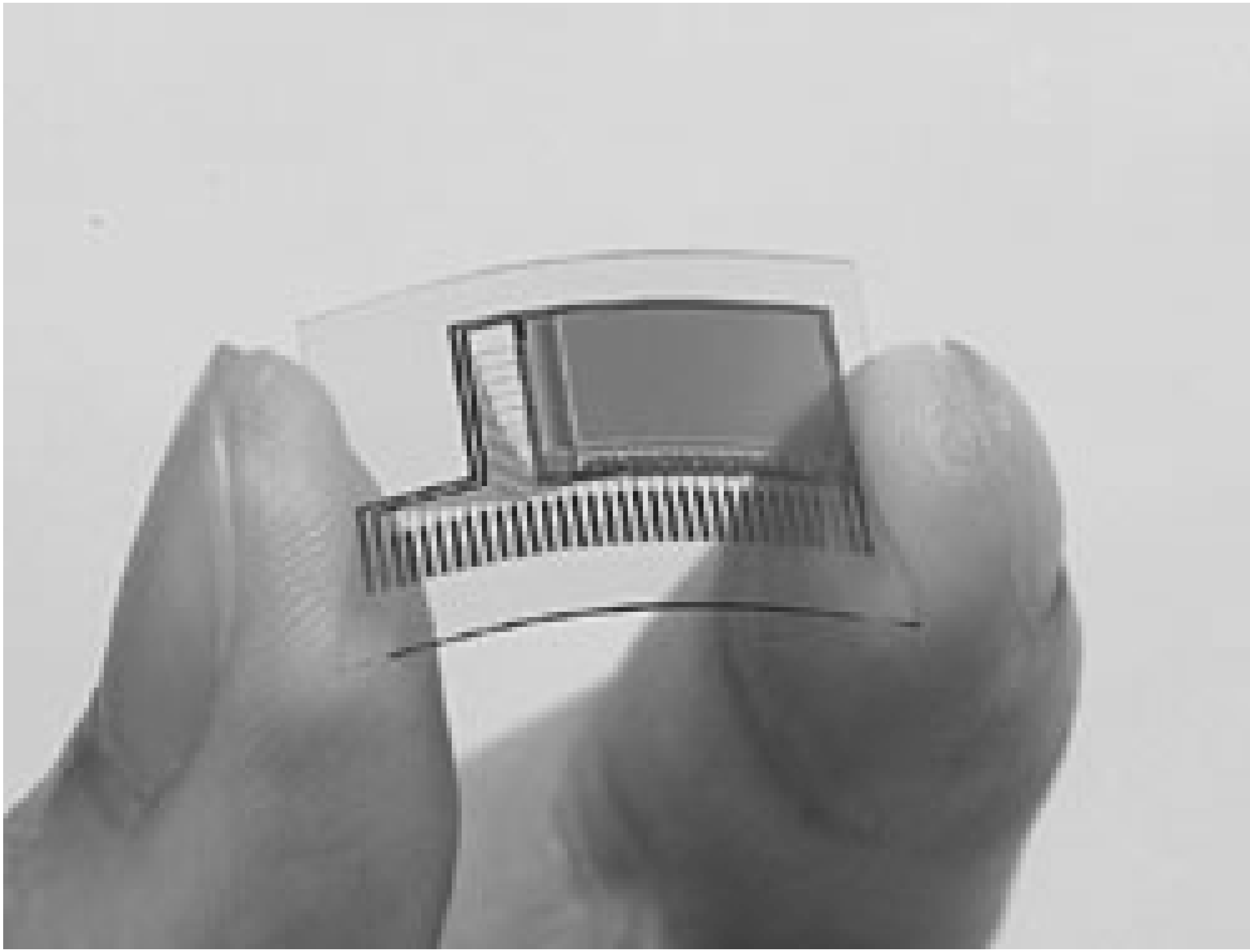



**写真2**
**非同期プロセッサの評価ボード**

LCD（液晶ディスプレイ）画面上に四つのアイコンが表示されている．それぞれ，テキスト編集，CPUによるビット・イメージ連続転送表示，電卓機能，DMAC（direct memory access controller）によるビット・イメージ連続転送表示などのデモンストレーションを実行する．ボード右下のボタン・スイッチは，左から順に[←]キー，[→]キー，[Enter]キー，[End]キー，[System Reset]キー，[LCD Reset]キーに相当し，上記のアプリケーションの選択，各アプリケーションのカーソル位置の制御，アプリケーションの終了などの制御に用いる．

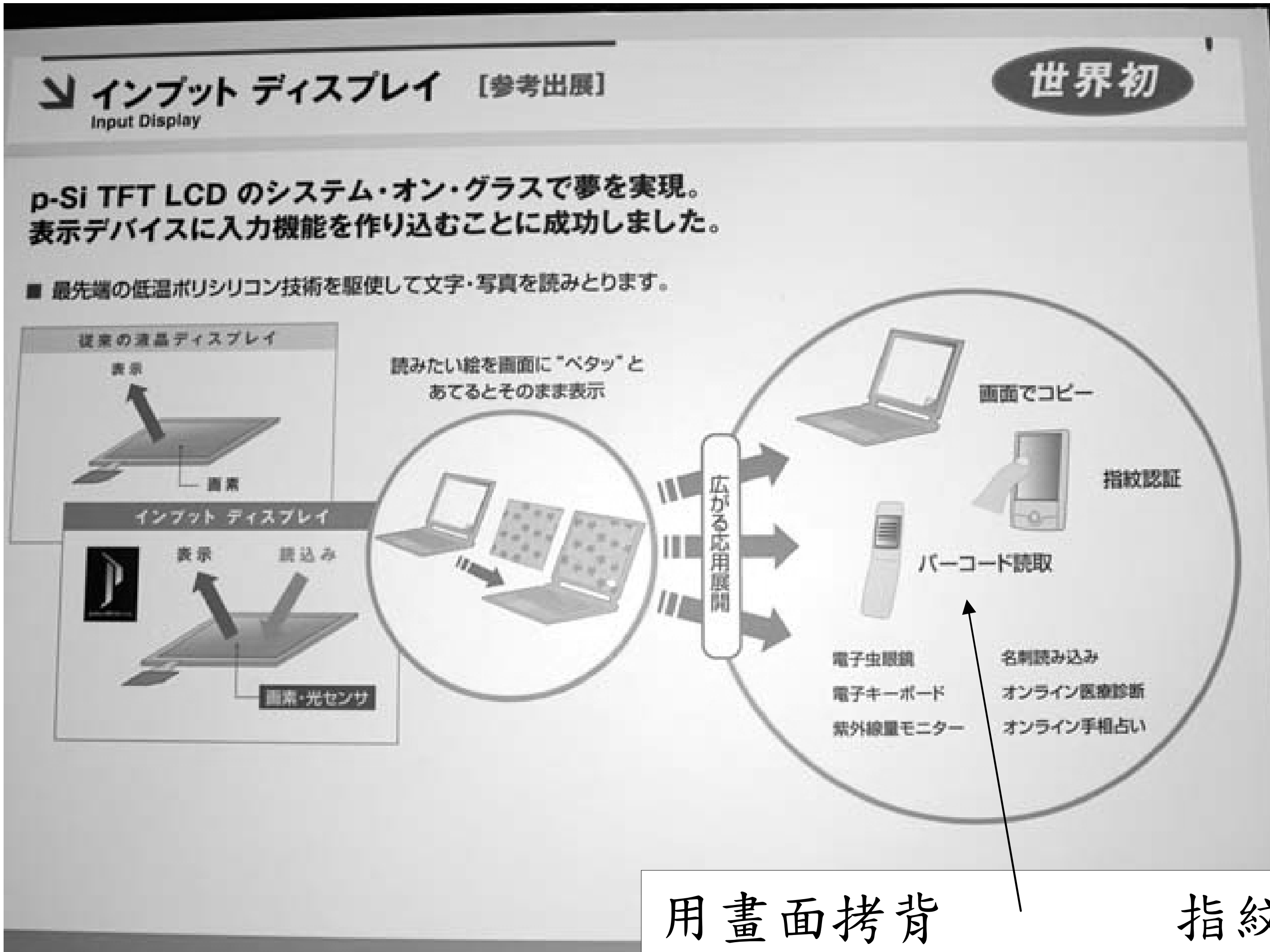
可撓之非同步CPU

Flexible SRAM by TFT on plastic
by EPSON(2005/9/29)



Toshiba 之 input display

-- 在製作TFT array 的同時將Photo diode做進array中




| | |
|---|---|
| 用畫面拷背 | 指紋認證 |
| 讀取條碼 | |
| 電子放大鏡 | 名片讀入 |
| 電子鍵盤 | 線上醫療診斷 |
| 紫外線量監控 | 線上手相算命 |


2005.9.20

# Si晶圓, SOI晶圓與玻璃基板製作法之比較

## Si晶圓

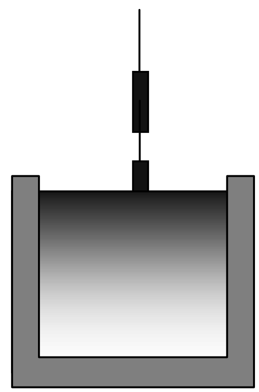
精鍊:

$SiO_2$(矽砂) + 2C → Si + 2CO (1800℃) : 2N

Si+3HCl→$SiHCl_3$+$H_2$（300℃）

$SiHCl_3$+$H_2$→Si(多晶)+3HCl（1100℃）: 11N

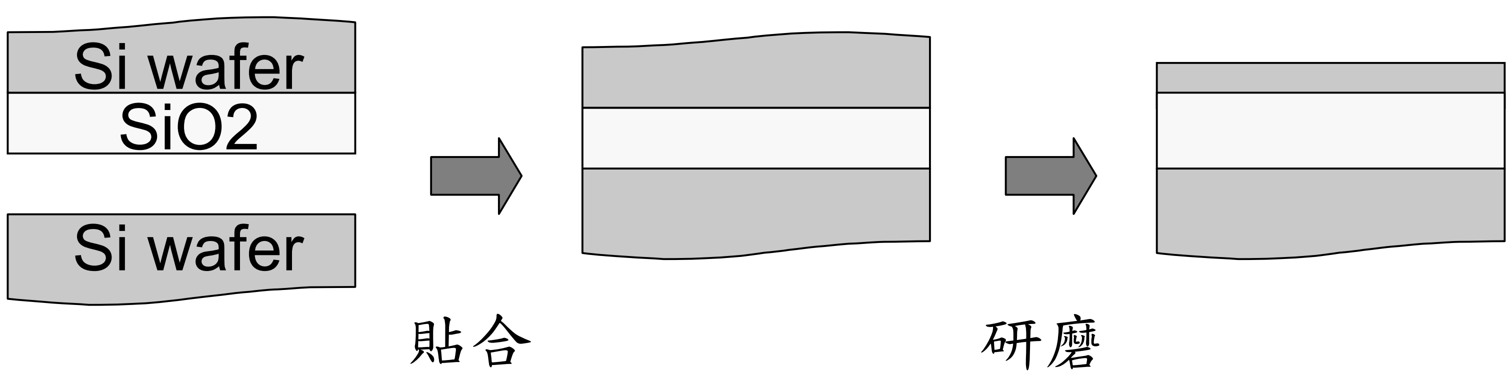
單晶化:



晶圓化:

切片 → 化學研磨
→物理研磨 → 鏡面研磨
→洗淨 → 包裝

## SOI晶圓



## TFT基板

玻璃基板形成

SiO2(矽砂) → Glass

Si/SiO2薄膜沉積

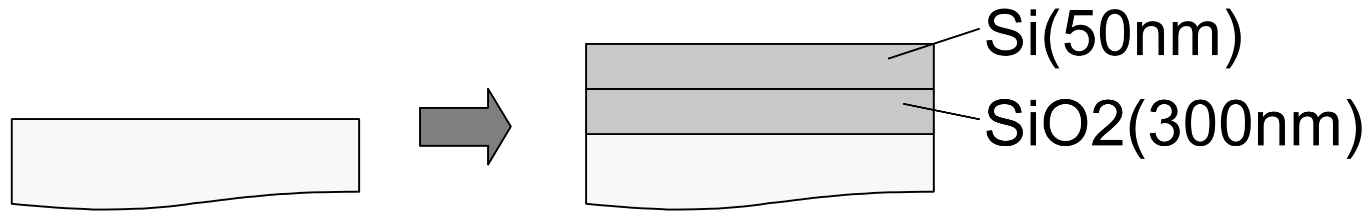


Table 1. Approximate amount of energy for manufacturing substrates (thickness: 0.7 mm).

| Substrate material | Energy ($kWhm^{-2}$) |
|---|---|
| Single-crystal silicon | 1000 |
| Fused quartz | 700 |
| Glass | 2 |

Table 2. Typical amount of energy needed for major fabrication steps (substrate thickness: 0.7 mm).

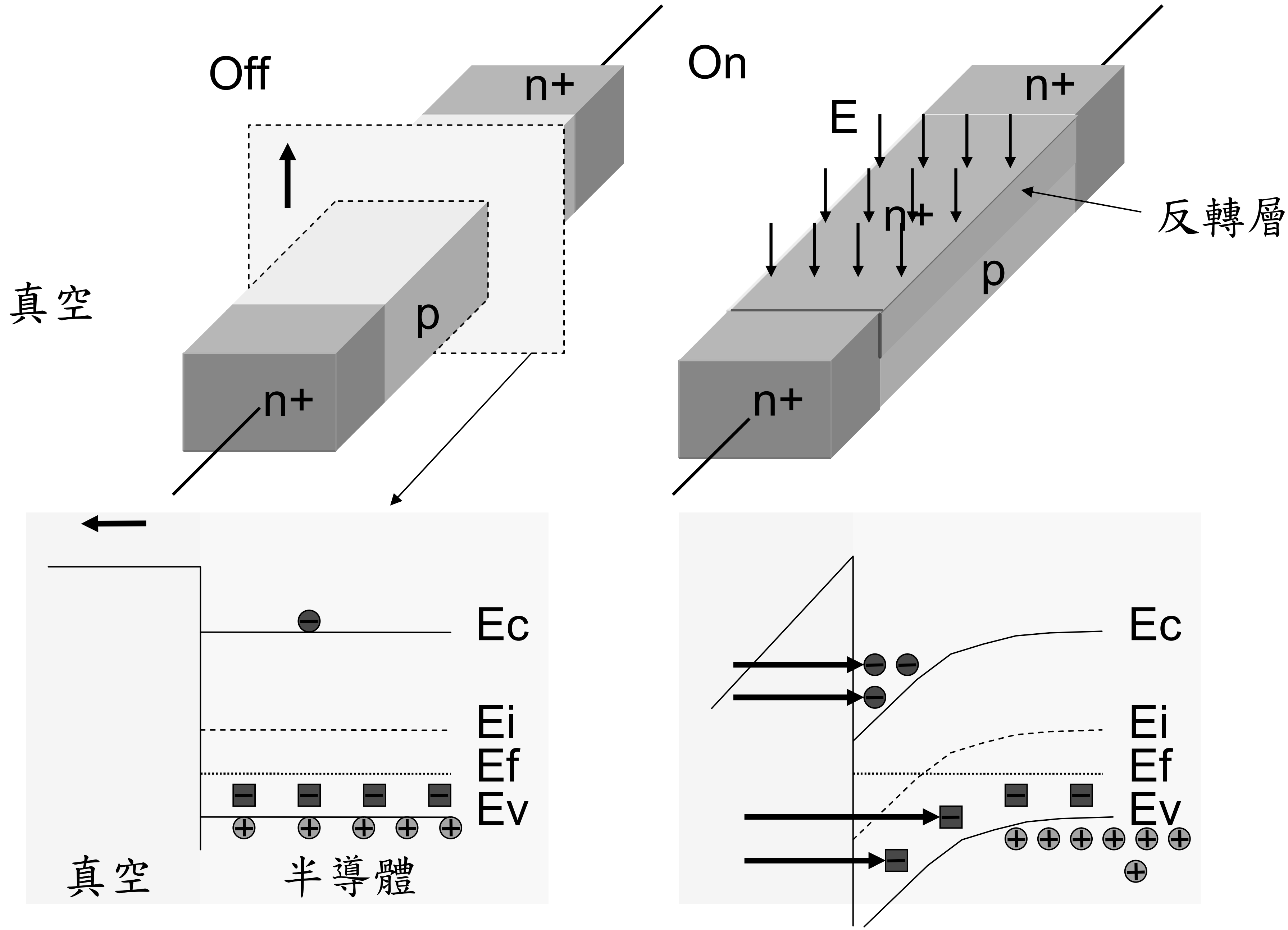
| Process step | Energy ($kWhm^{-2}$) |
|---|---|
| Amorphous Si thin-film deposition using LPCVD | 5~10 |
| Solid-state crystallization of silicon thin film (600 C, 15 h) | ~10 |
| Excimer laser annealing | ~2 |
| Sputter thin-film deposition | 5~10 |

TFT積體電路之製造所需能量僅為LSI之1/100

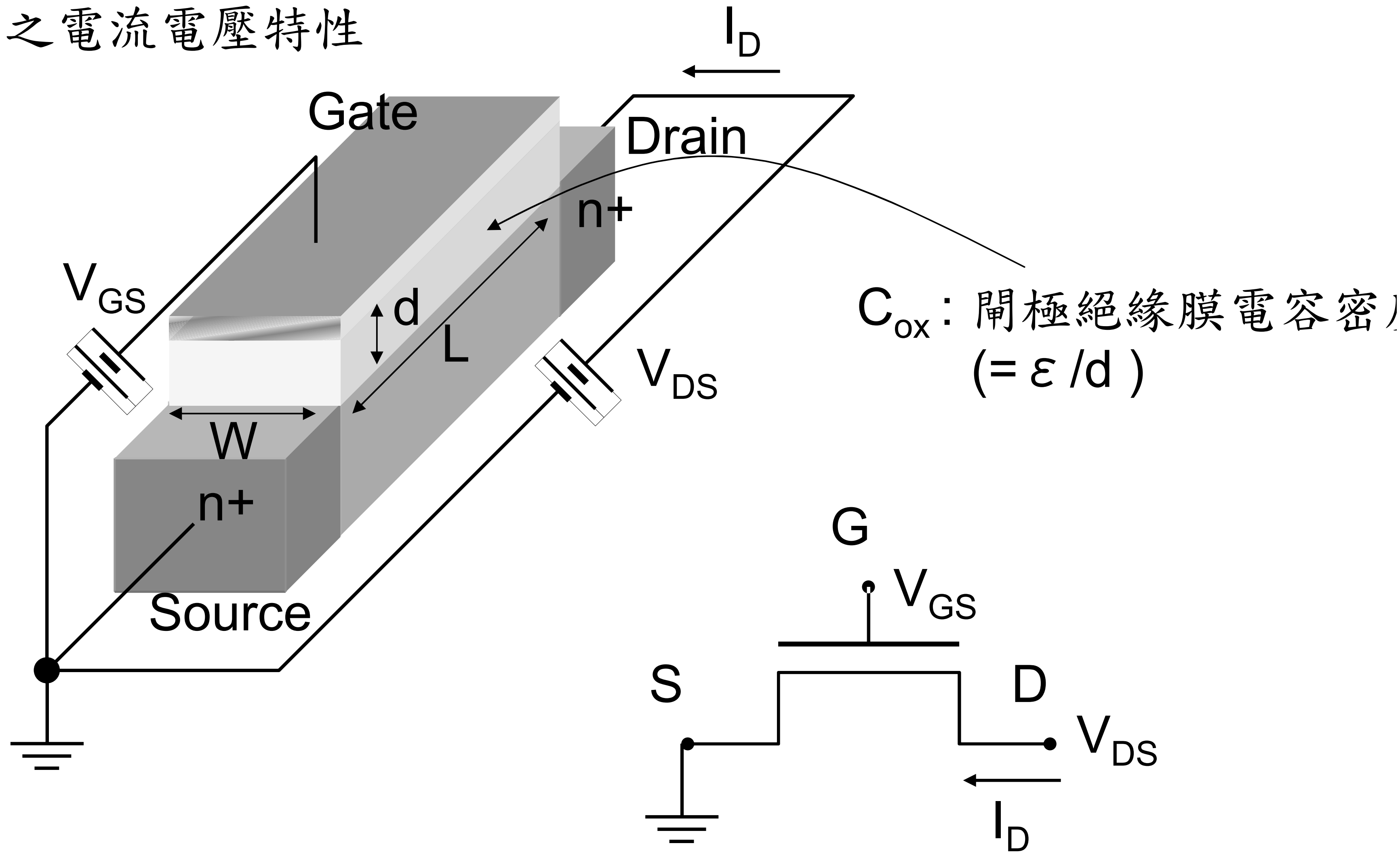
| | 矽晶圓 | 玻璃基板 |
|---|---|---|
| 基板面積 | 324～729cm2 | 4464～6716cm2 |
| 處理溫度 | 900～1200度 | 最高500度（省能） |
| 電晶體結構 | bulk Si | SOI結構 |
| | Poly gate | Metal gate(高速) |
| CMOS製程 | 不易 | 容易 |
| Scaling | 10n-100nm | 0.5$\mu$-3$\mu$ |

# MOS電晶體元件物理

# FET (Field Effect Transistor) 之原理

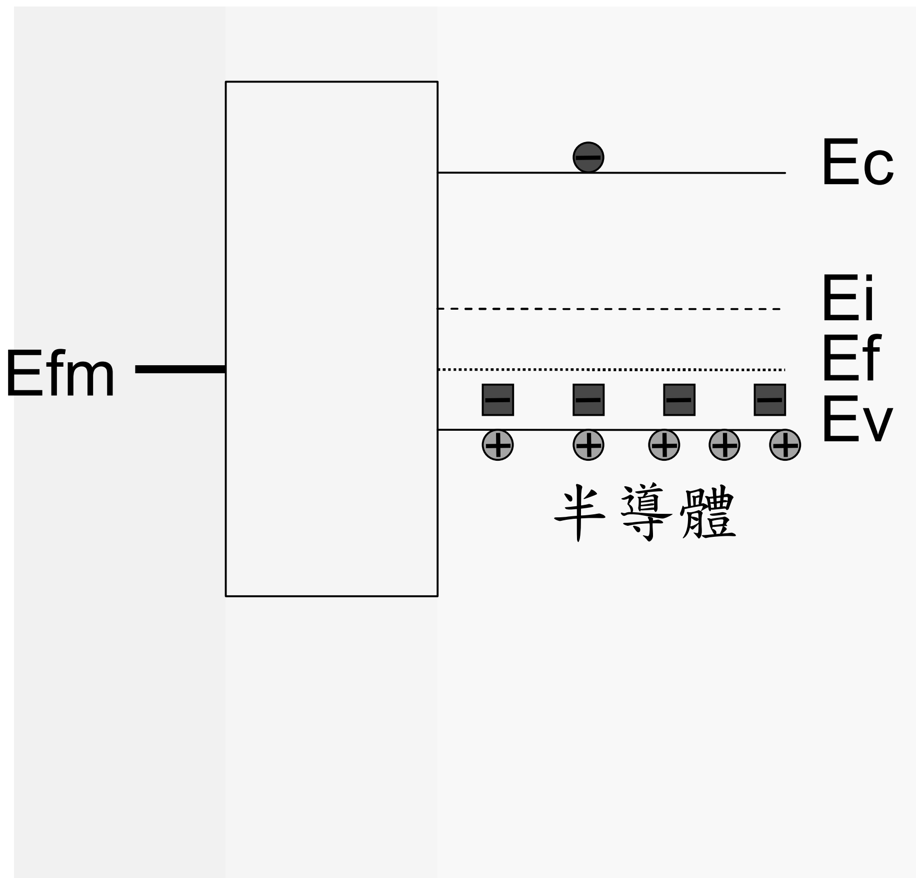


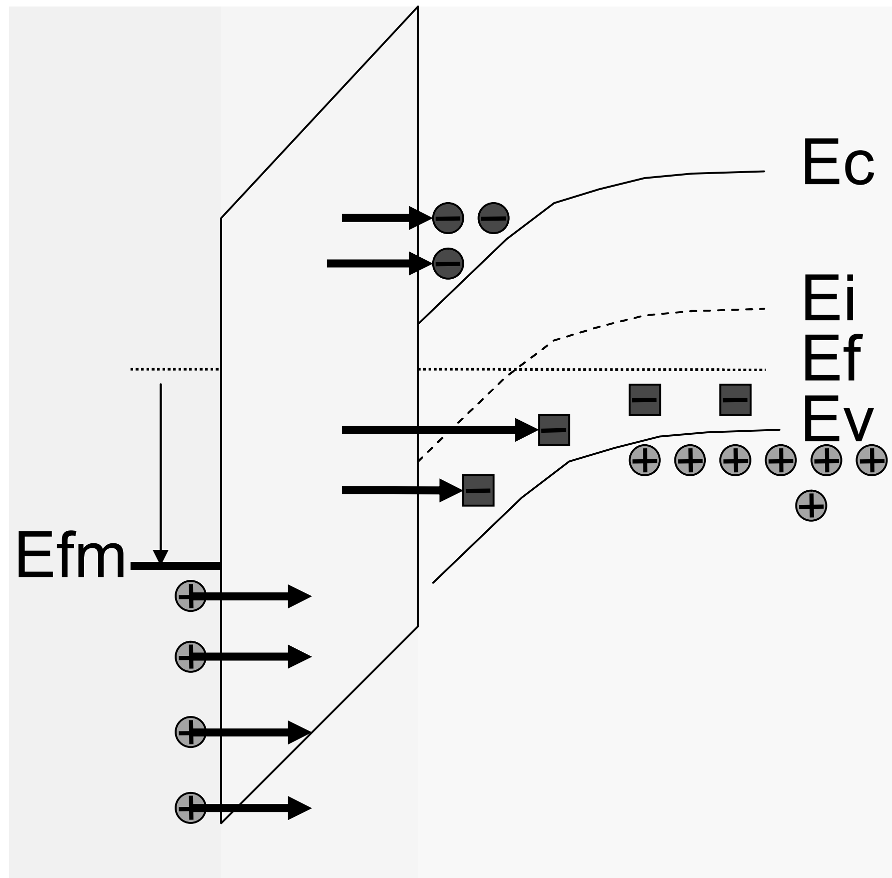
# FET 之電流電壓特性

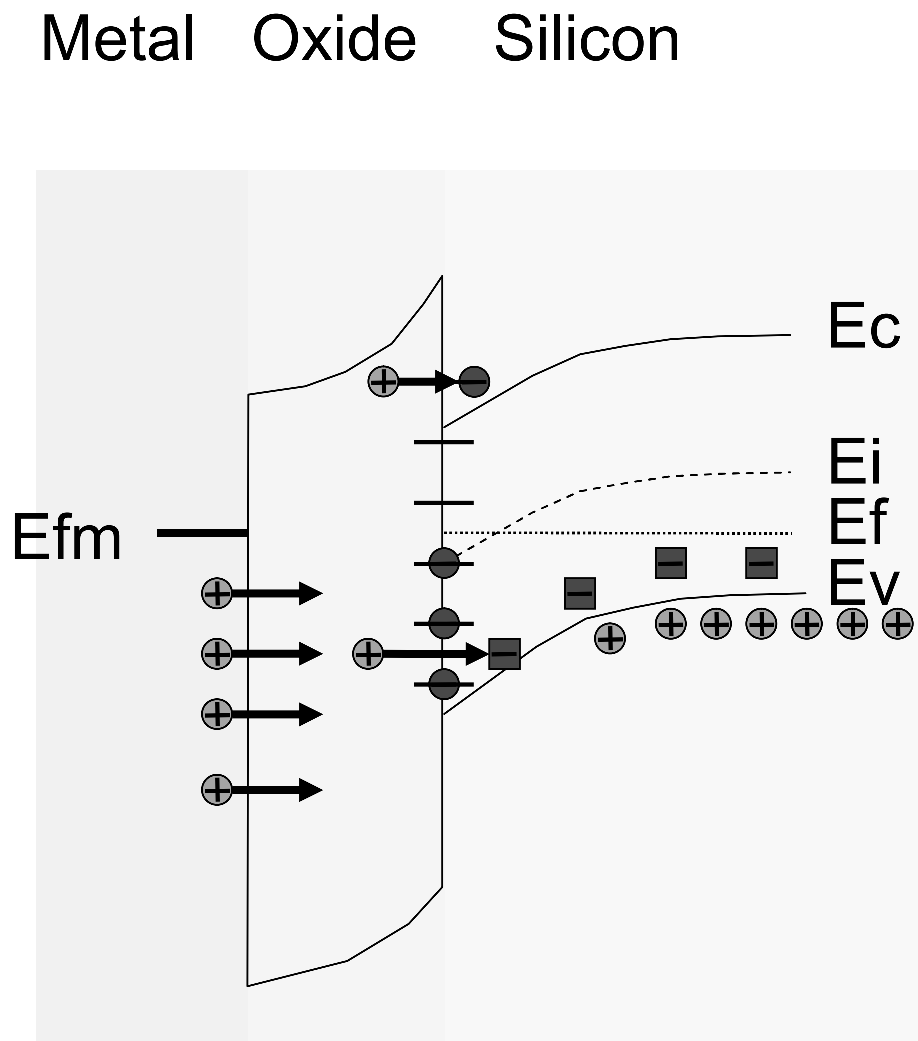



Characterization : $I_{D}$-$V_{GS}$ ,$I_{D}$-$V_{DS}$

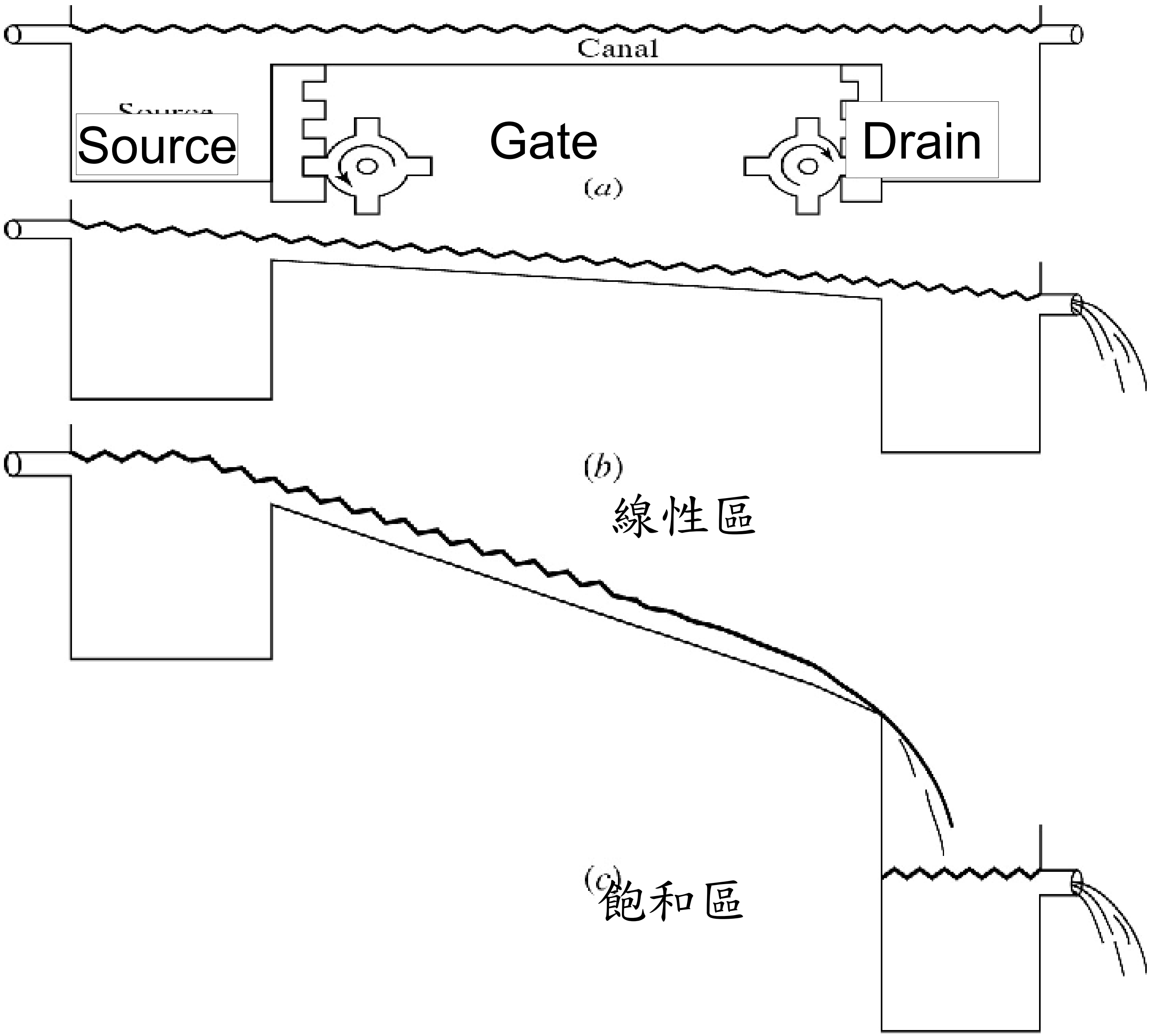
Metal Oxide Silicon



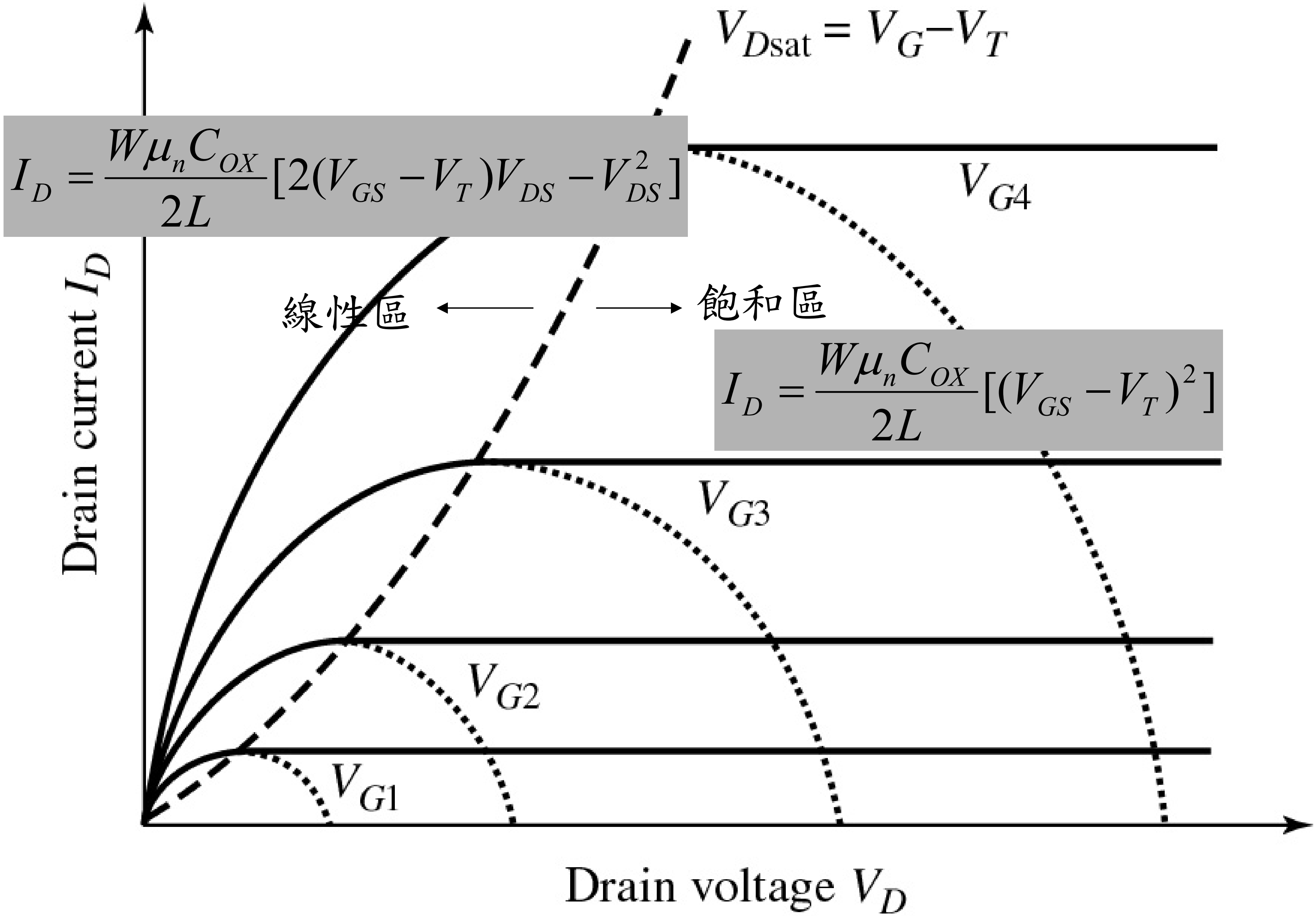






絕緣膜對Vt之不確定性影響: 膜中電荷+界面陷井

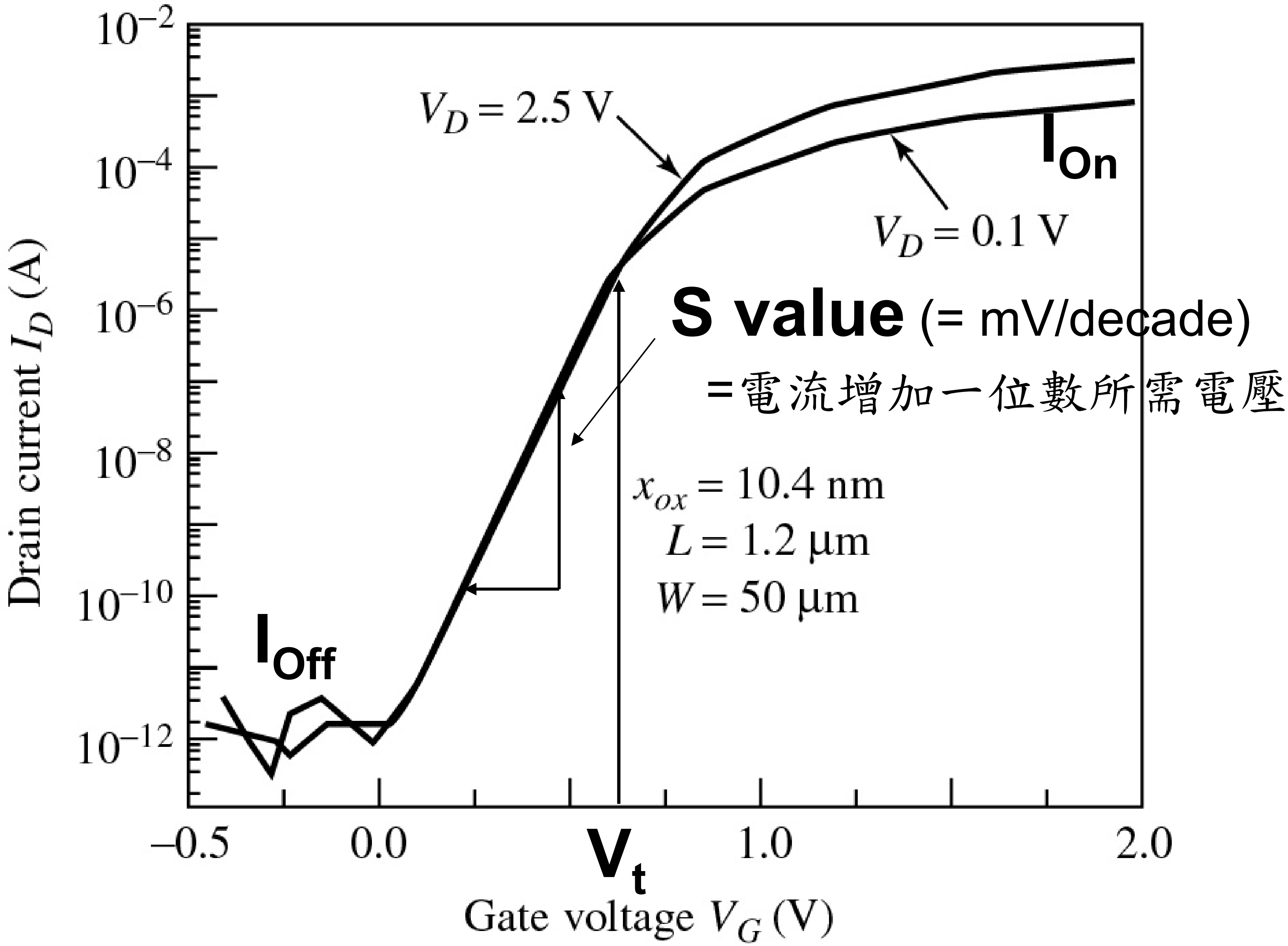


Canal
Source
Gate
Drain
(a)
(b)
線性區
(c)
飽和區



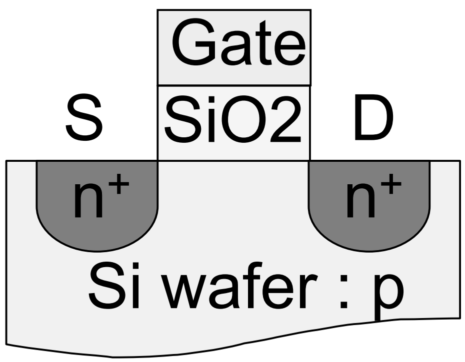
$V_{Dsat} = V_G - V_T$
$I_D = \frac{W\mu_n C_{OX}}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$
$V_{G4}$
線性區
飽和區
$I_D = \frac{W\mu_n C_{OX}}{2L}[(V_{GS} - V_T)^2]$
$V_{G3}$
$V_{G2}$
$V_{G1}$
Drain current $I_D$
Drain voltage $V_D$

# Subthreshold charasteristics of a MOS transistor



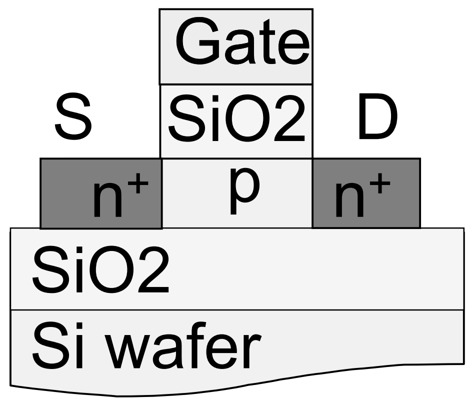
## Structure of MOS Transistor

### 1. Bulk MOS



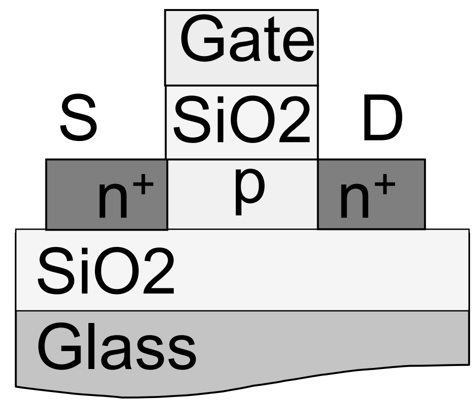

現今LSI

### 2. SOI MOS
(Si On Insulator)




次世代 LSI

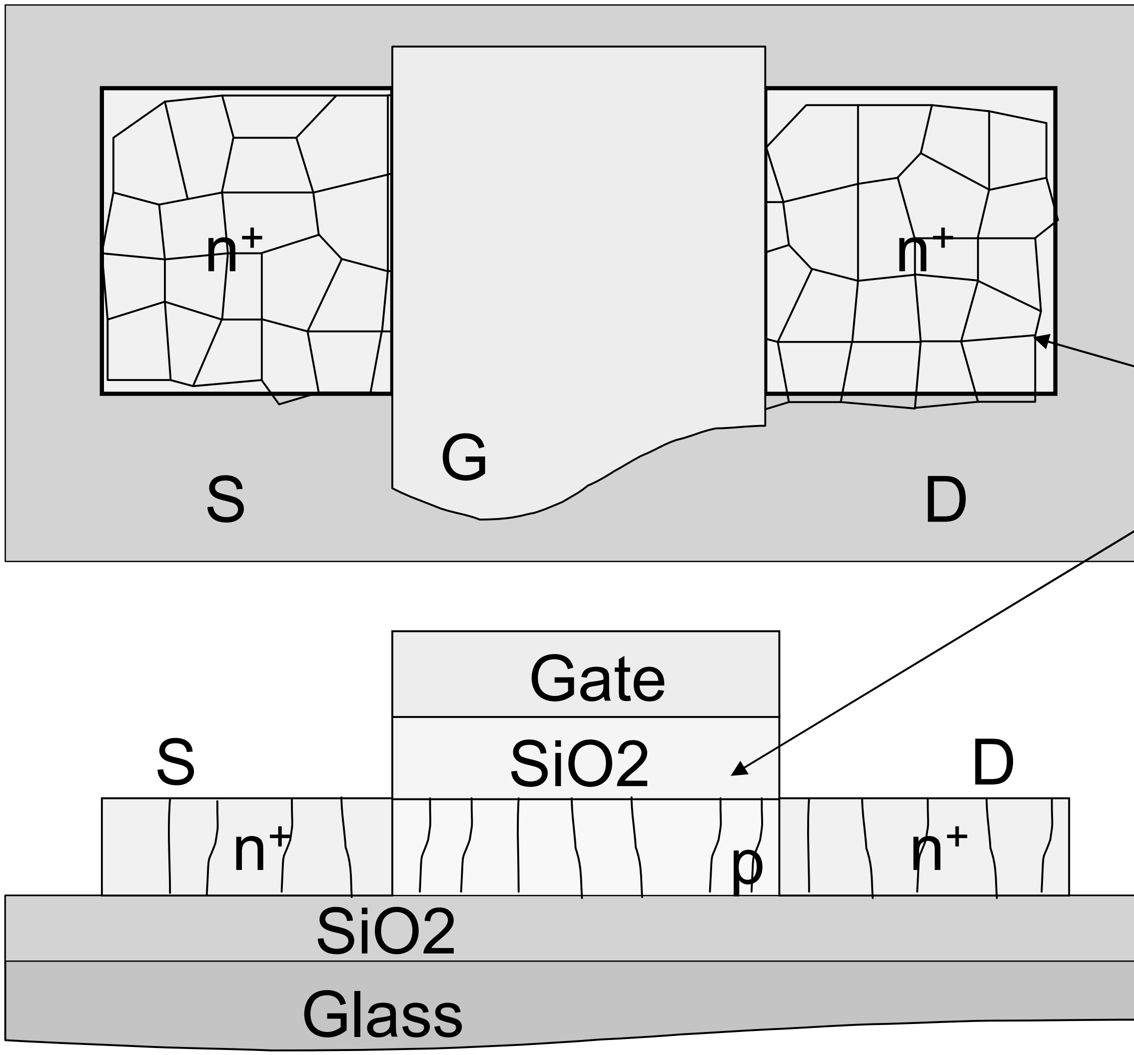
### 2. TFT MOS




現今TFT-LCD
Or TFT-OLED
(LTPS)

相同結構

# LTPS-TFT結構




與SOI-MOS
比較下之問題點:

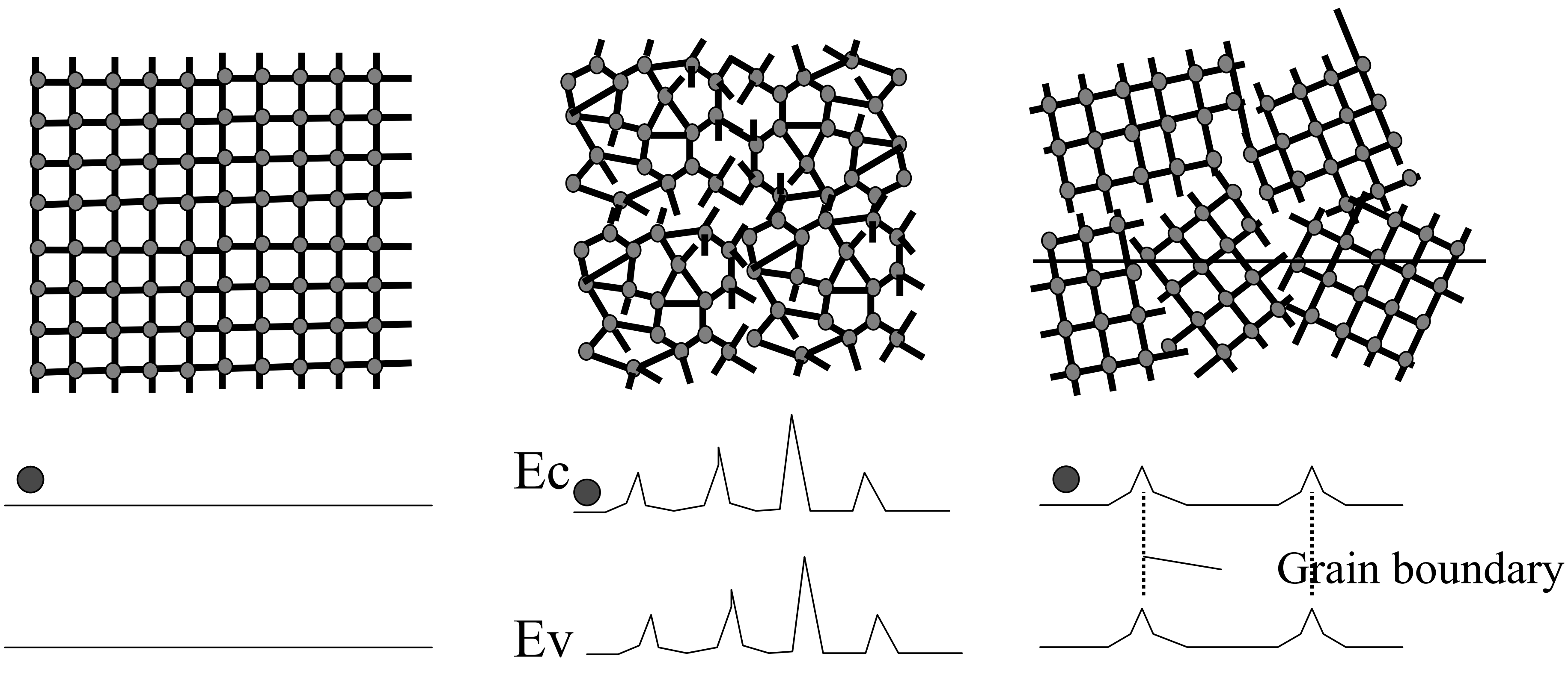
1. Poly-Si film
2. SiO2 gate oxide

# Mobility of Si film

1. c-Si (crystalline, 單晶)

2. a-Si (amorphous, 非晶)

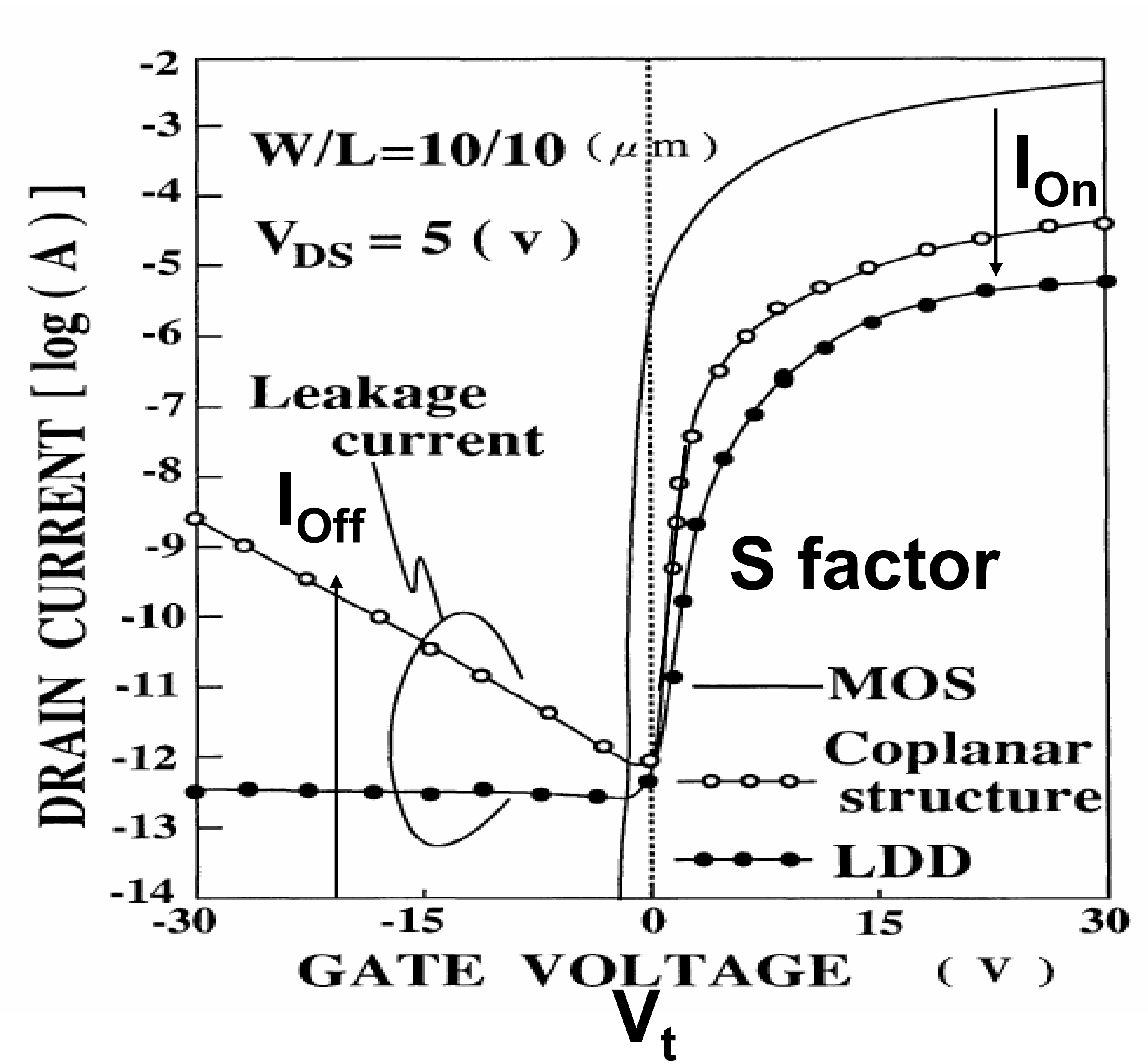
3. poly-Si (polycrystalline, 多晶)




> 500 cm2/vs

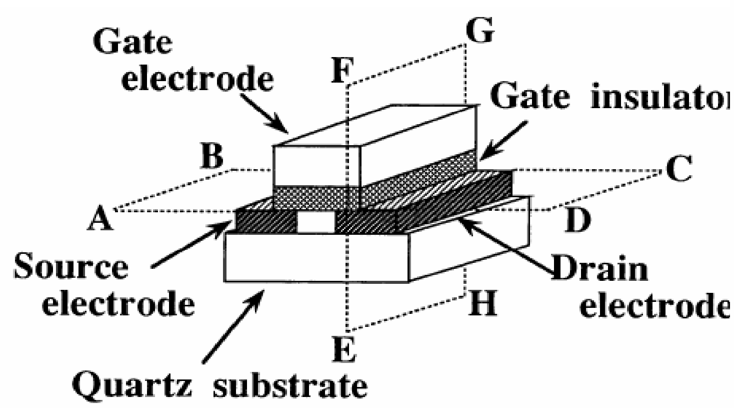
Mobility: < $1 cm^2/vs$

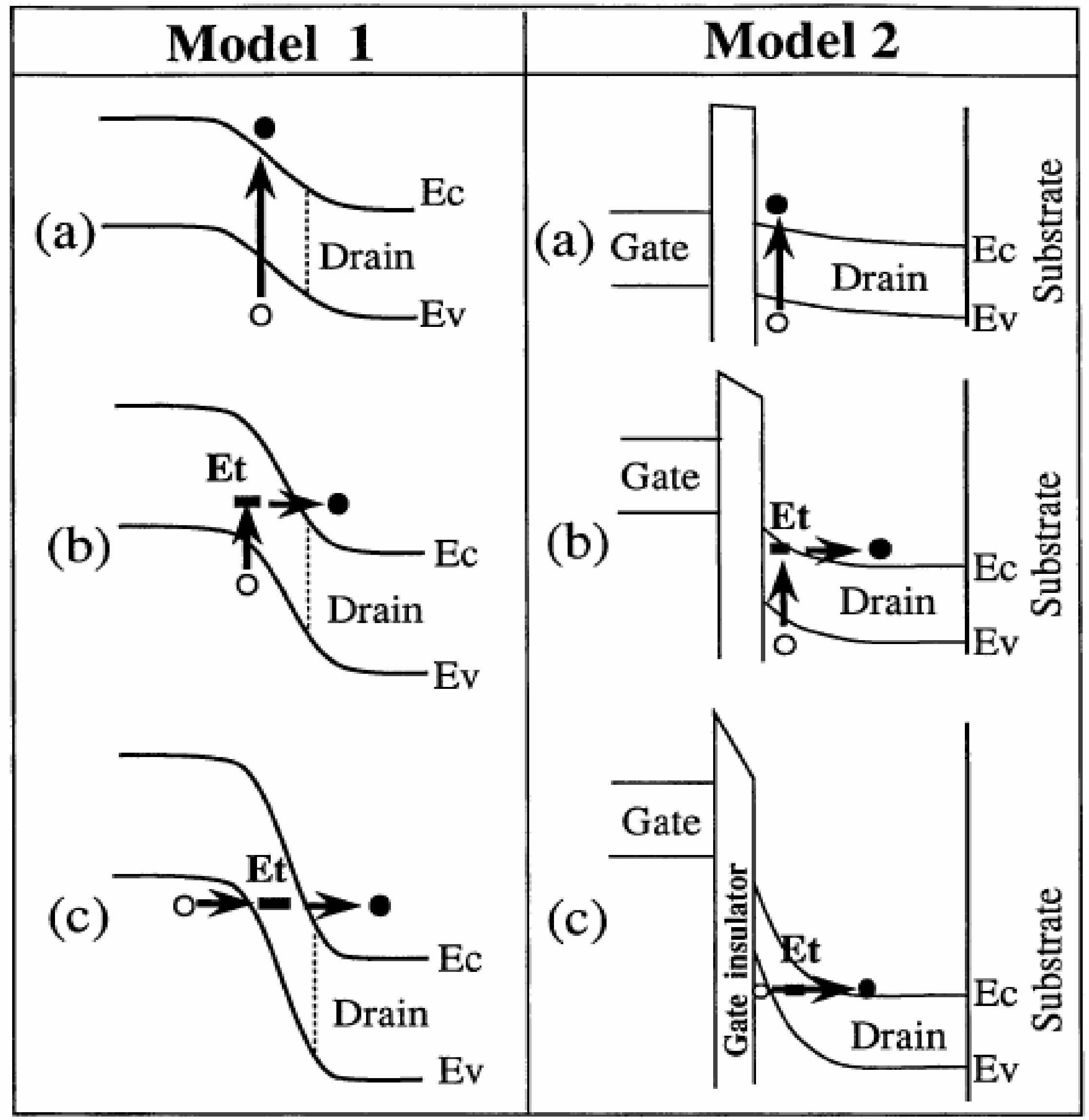
$10 \sim 500\ cm^2/vs$



W/L=10/10 (μm)
V_DS = 5 (v)
I_On
Leakage current
I_Off
S factor
MOS
Coplanar structure
LDD
DRAIN CURRENT [ log (A) ]
GATE VOLTAGE (v)
V_t

## Ioff之原因


Gate
electrode
F
G
Gate insulator
B
C
A
D
Source
electrode
Drain
electrode
H
E
Quartz substrate


Model 1
Model 2
(a)
Ec
Drain
Ev
(b)
Et
Ec
Drain
Ev
(c)
Et
Ec
Drain
Ev
(a)
Gate
Drain
Ec
Ev
Substrate
(b)
Gate
Et
Ec
Drain
Ev
Substrate
(c)
Gate
Gate insulator
Et
Ec
Drain
Ev
Substrate

TFT特性變因

Ion下降: → mobility 下降

→ 1. polycrystalline structure

2. SiO2/Si interface trap

Ioff上昇: → Field emission current → Polycrystalline structure

Vt變化: → SiO2 charge, SiO2/Si interface trap

S值上升: → SiO2/Si interface trap

最關鍵技術:

1. 矽膜結晶性 2. 絕緣膜品質

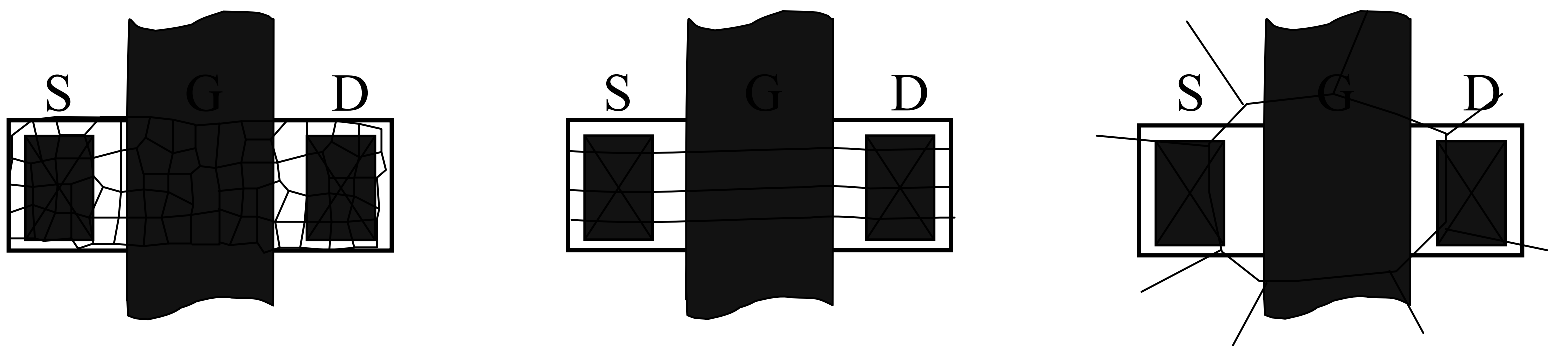
# 3. 次世代LTPS-TFT之研發

# LTPS-TFT未來研發重點

1. 矽膜結晶性　　　2. 絕緣膜品質

[redacted]

a)電晶體之單晶化




1G TFT

2G TFT
Lateral growth

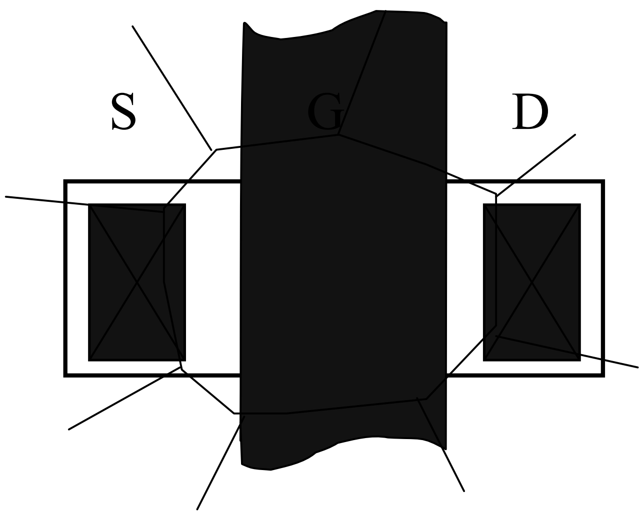
3G TFT
Single grain

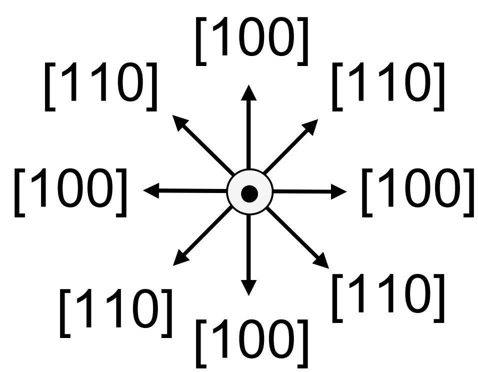
⇨ (1)結晶位置控制技術
(2)結晶粒徑增大技術

b)結晶粒內缺陷之降低

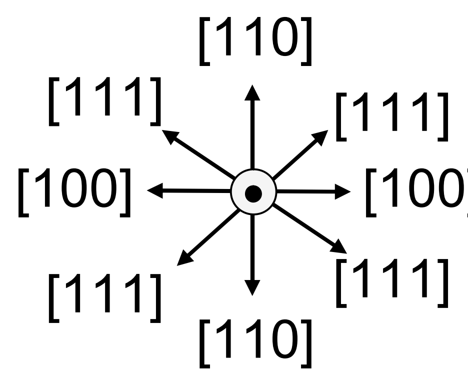
⇨ 結晶粒徑增大技術之開發 (近平衡狀態下長晶)

c)結晶方位之控制(表面方位, 面內方位)



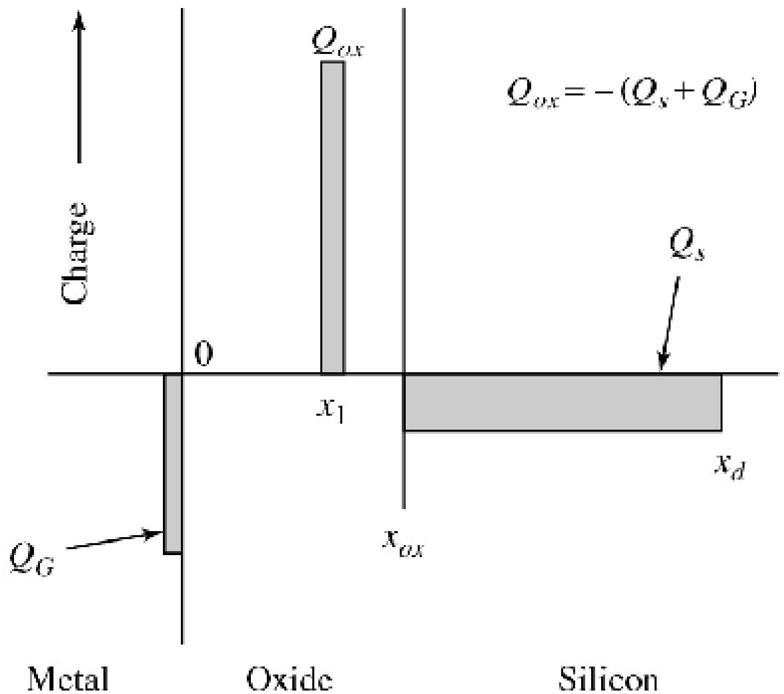




(100)



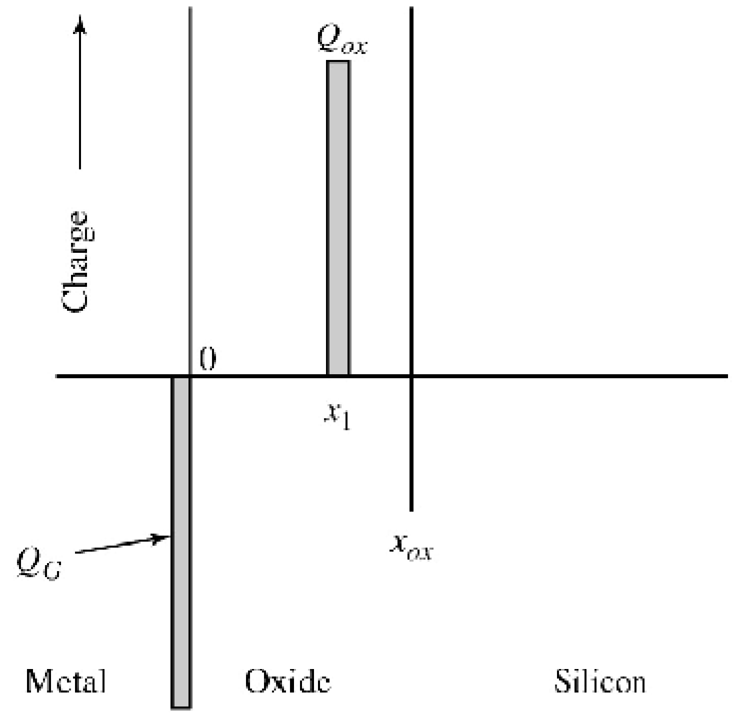

(110)

# 2. 絕緣膜品質



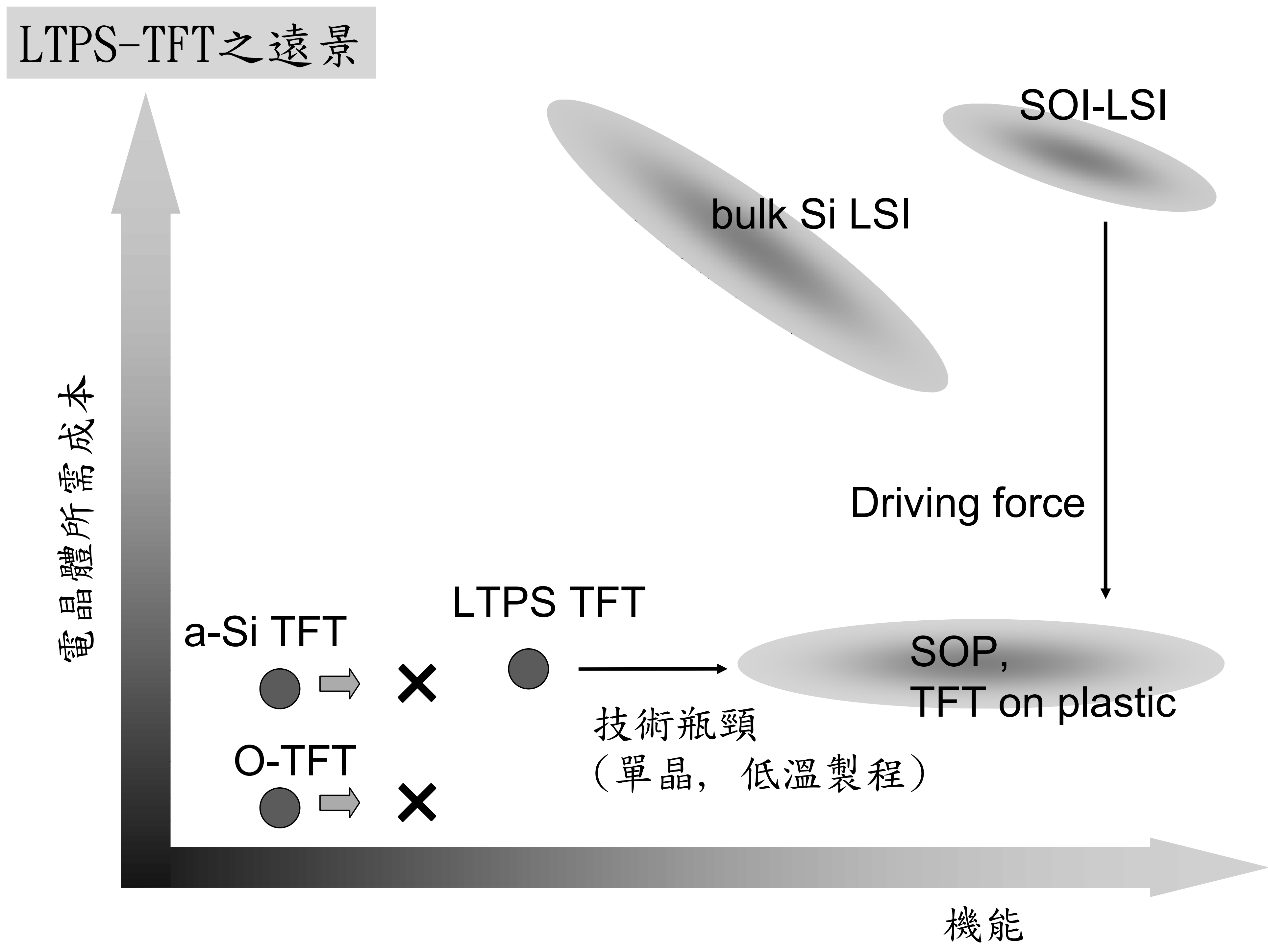
Charge
$Q_{ox}$
$Q_{ox} = -(Q_s + Q_G)$
$Q_s$
0
$x_1$
$x_d$
$x_{ox}$
$Q_G$
Metal
Oxide
Silicon


(a)



Charge
$Q_{ox}$
0
$x_1$
$x_{ox}$
$Q_G$
Metal
Oxide
Silicon

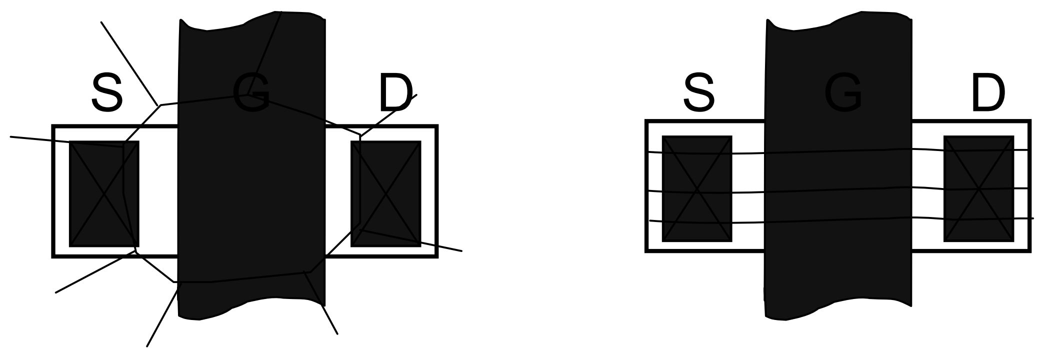

(b)


LTPS-TFT之遠景
電晶體所需成本
機能
SOI-LSI
bulk Si LSI
Driving force
LTPS TFT
a-Si TFT
O-TFT
SOP,
TFT on plastic
技術瓶頸
(單晶，低溫製程)

SOP (System on panel)

High mobility & uniformity TFT is demanded

⇨ Single grain TFT or lateral grain TFT




Following technics are demanded in ELC process

1. Grain location control

   Grains can be located at the positions for TFTs

2. Grain size enlargement

   - Grain can surpass the channel dimension
   - Better crystallinity (equilibrium grain growth)

# Fabrication methods for poly-Si film

[redacted]

H-diluted PECVD, cat-CVD···
$\mu$<100cm$^2$/vs, (111) faced

→ Low cost, but low performance

[redacted]

MILC+ELA (CGS)
$\mu \sim$ 300cm$^2$/vs, (110) faced

→ Applicable to 2nd generation TFT, but difficult for 3rd generation

[redacted]

$\mu \sim$ 500cm$^2$/vs, random faced

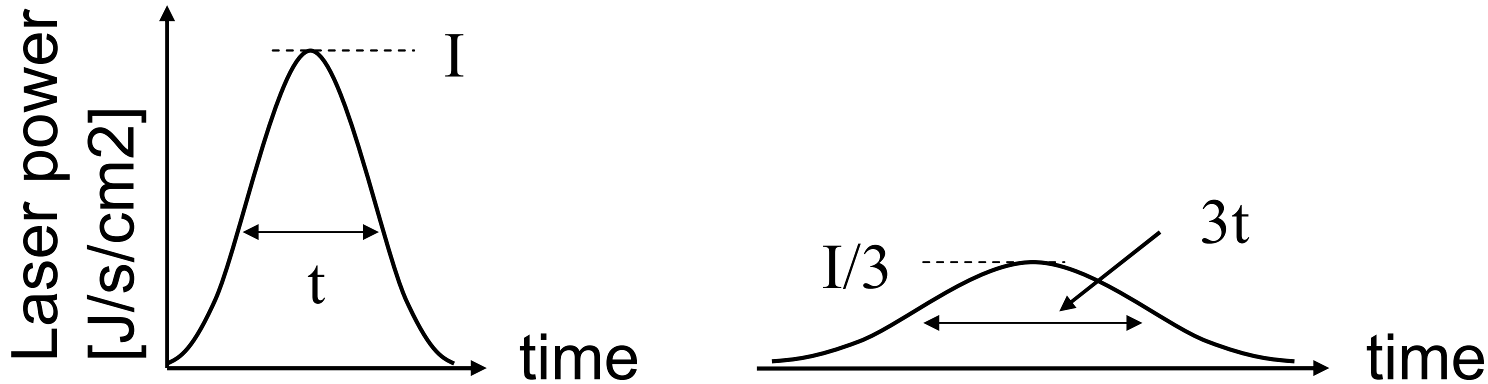
→ Applicable to 1st to 3rd generation TFT
Si film on plastic is also applicable

# 矽膜之雷射退火結晶化技術介紹

對退火光源之選擇:

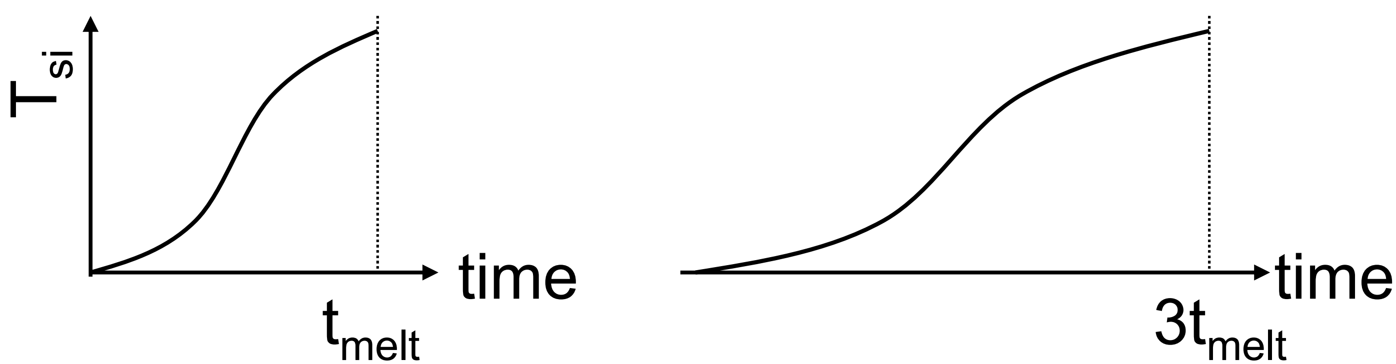
1. 脈衝幅之影響

不考慮熱量外流之損失時:




→ 總能量E相等

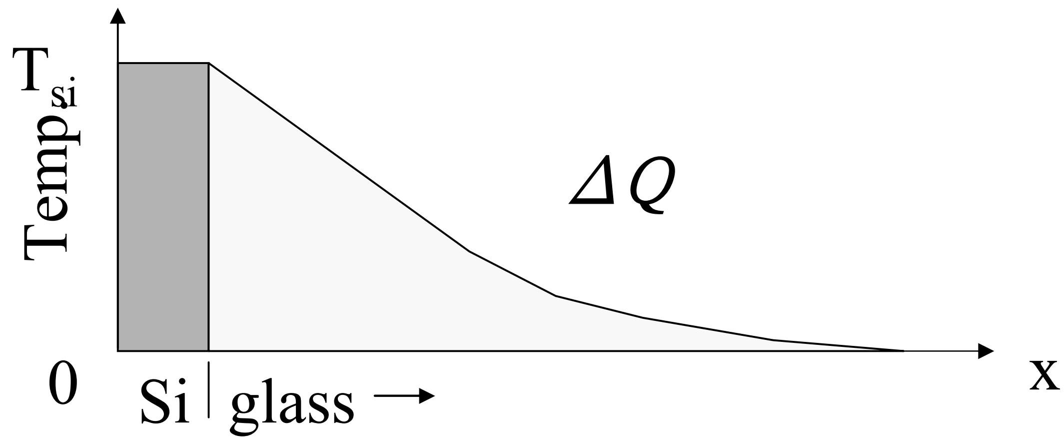
矽膜溫度$T_{si}$之變化:



考慮熱量外流之損失時:

擴散損失 $Q_d$:

$$Q_d \propto \sqrt{t_{melt}}$$




輻射損失 $Q_r$:

$$Q_r \propto t_{melt}$$

雷射融化矽膜所需能量 I:

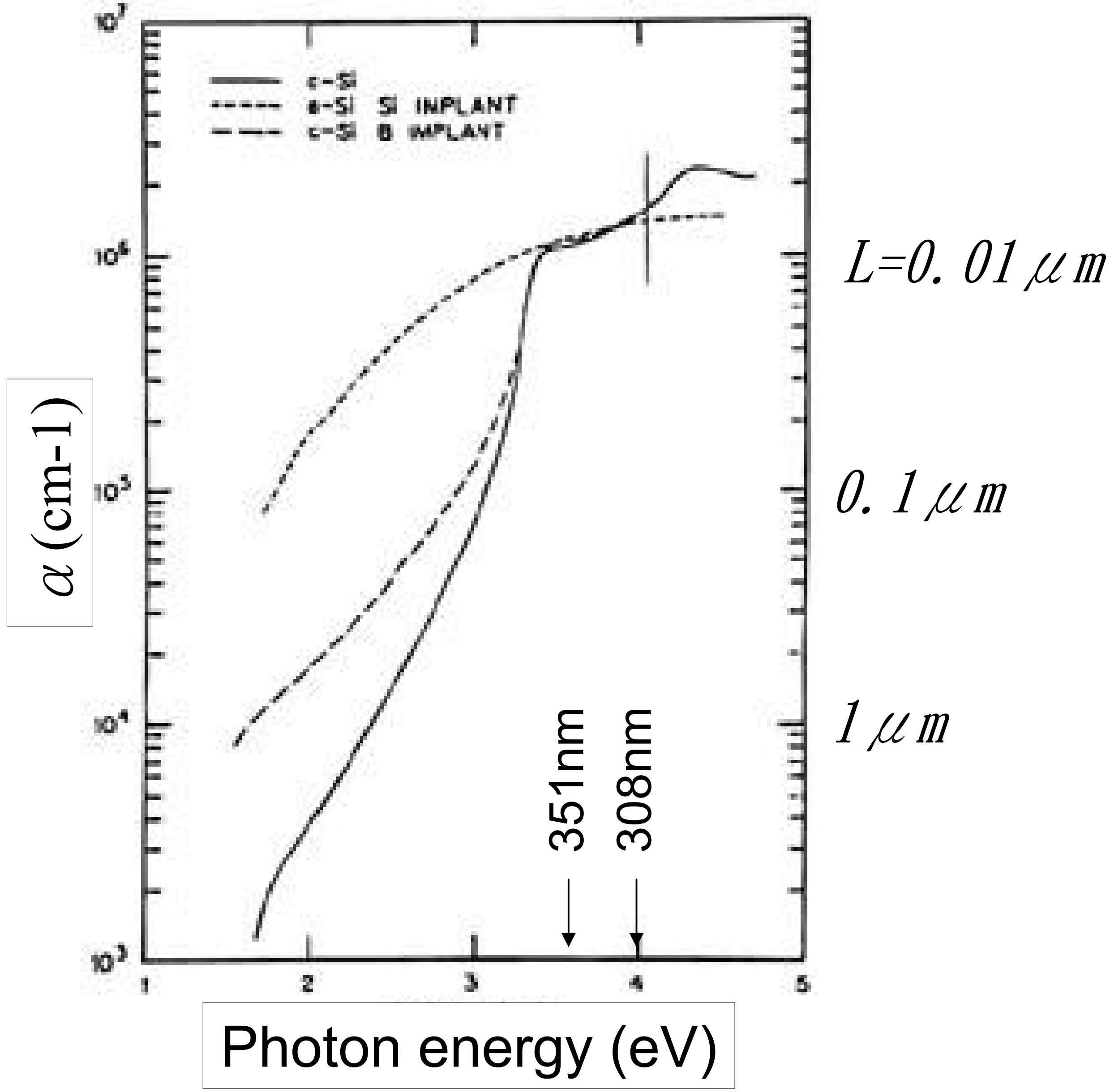
$$I = E + A_1 \sqrt{t_{melt}} + A_2 t_{melt}$$

→ 雷射光脈衝越短, 效率越高

對於脈衝短度之限制: 矽膜表層之蒸發

# 2.雷射波長λ之影響

$I = I_0 exp(-\alpha x)$  Absorption depth $L = 1/\alpha$



目前之準分子雷射光源

Wave length:

ArF: 193nm, KrF : 248nm, XeCl: 308nm, XeF: 351nm

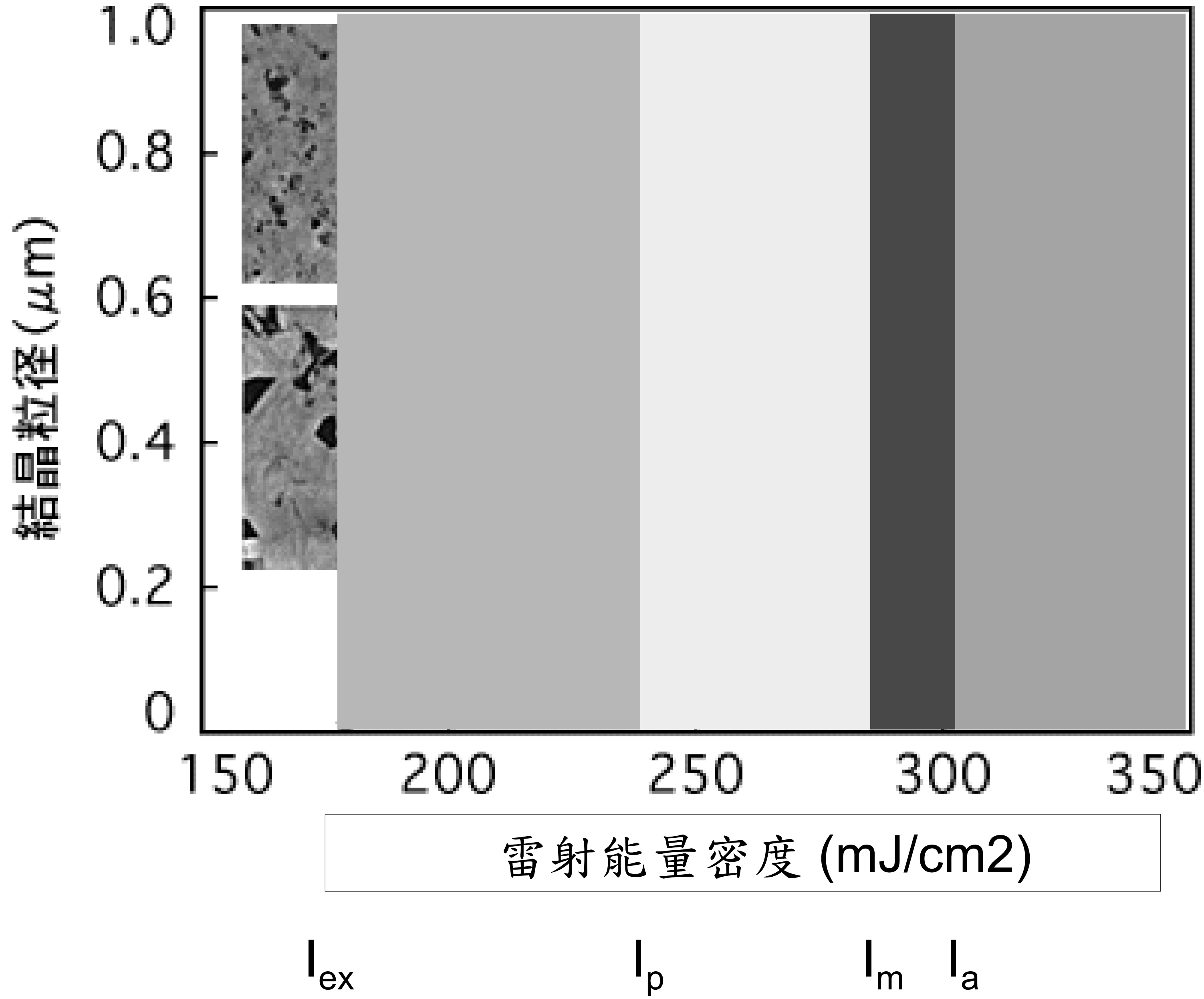
Pulse duration: 20ns ~ 50ns

Energy density: 100 ~ 1000mJ/cm2

Absorption depth : ~ 10nm

TFT之矽膜厚度約50 ~ 200nm

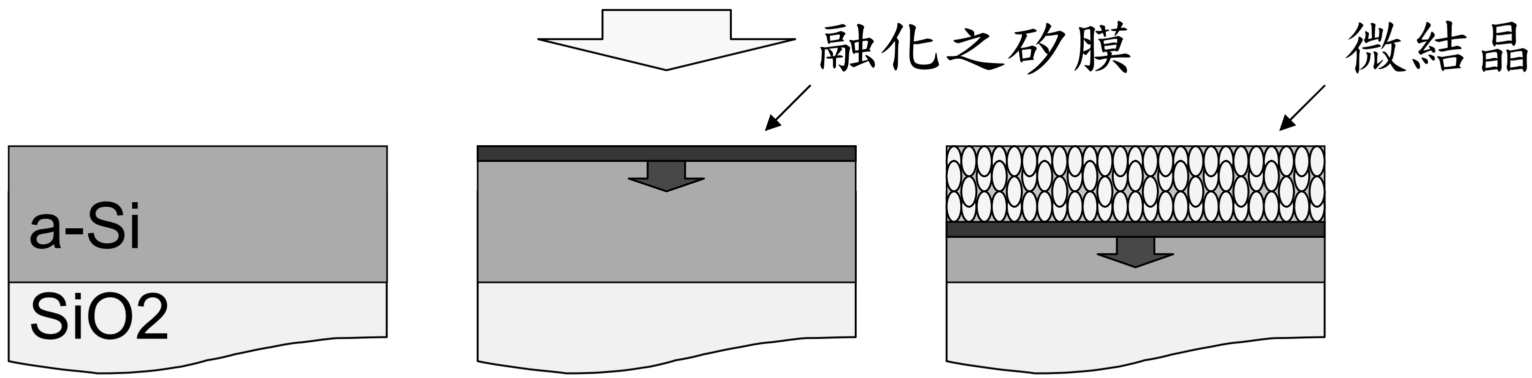
# 單發雷射照射能量密度對結晶粒徑之影響



矽膜雷射退火之結晶化機構

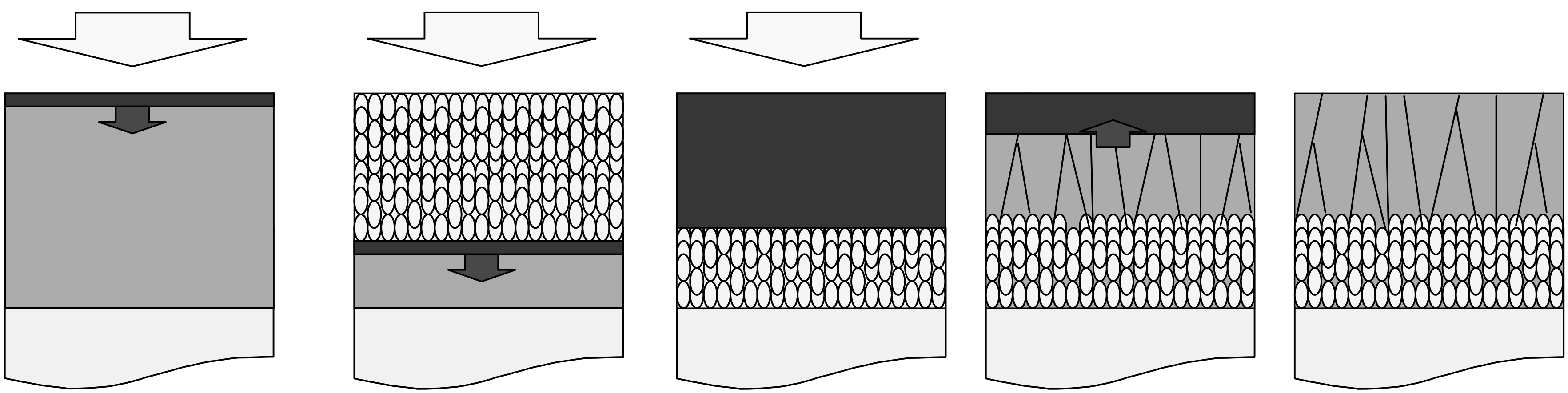
1. Explosive crystallization (爆炸性結晶化)

能量密度 : $I_{ex} \sim I_p$



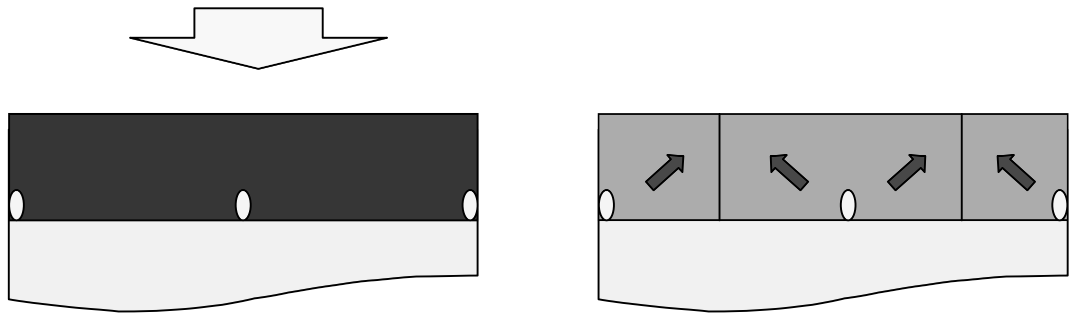
## 2. Partially melt (部份融化)

能量密度：$I_p \sim I_m$



1.表面融化　2.爆炸結晶　3.二次融化　4.長晶

能量密度接近 $I_m$



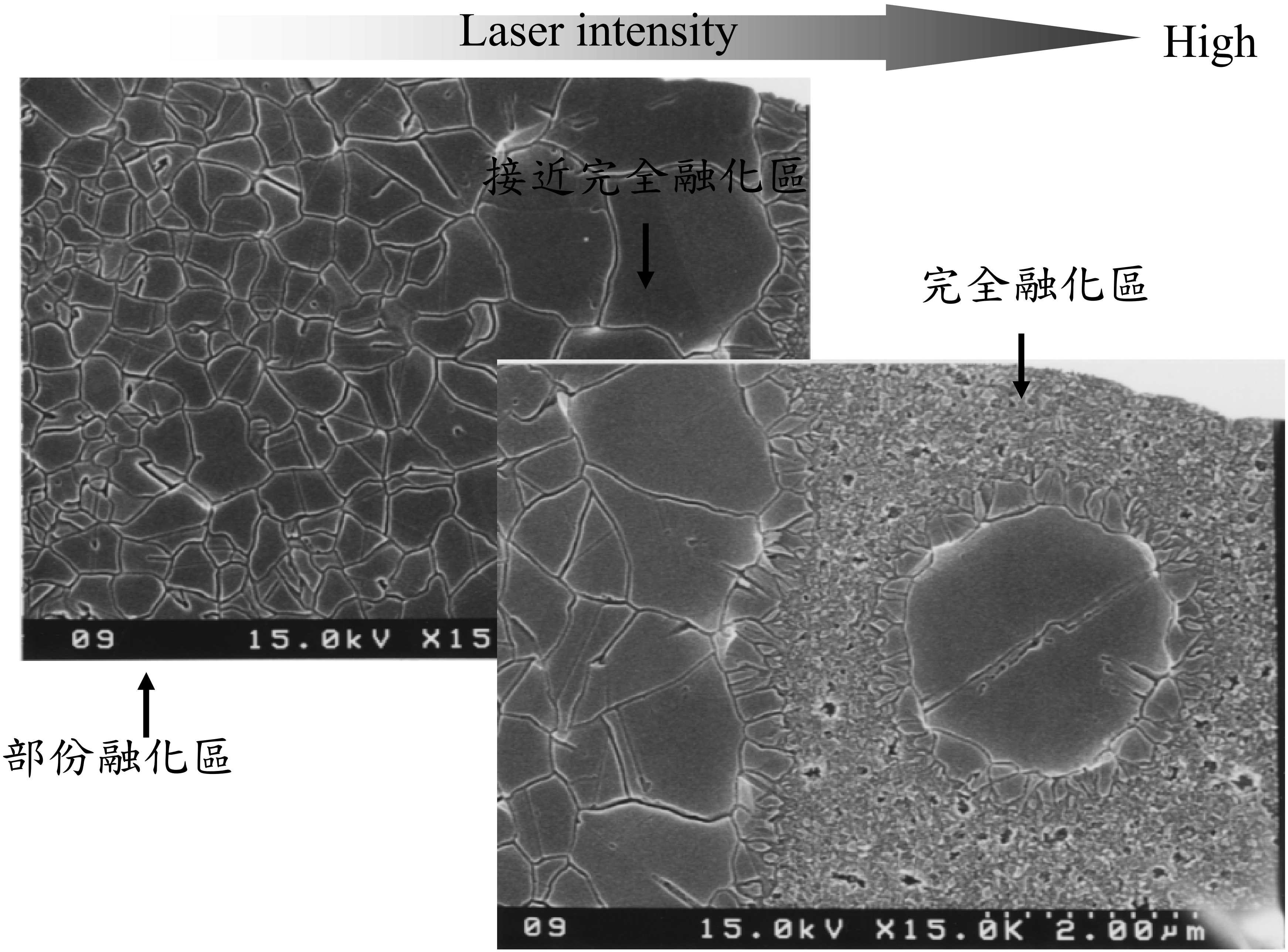
Lateral growth (橫向長晶)

## Completely melt (完全融化)

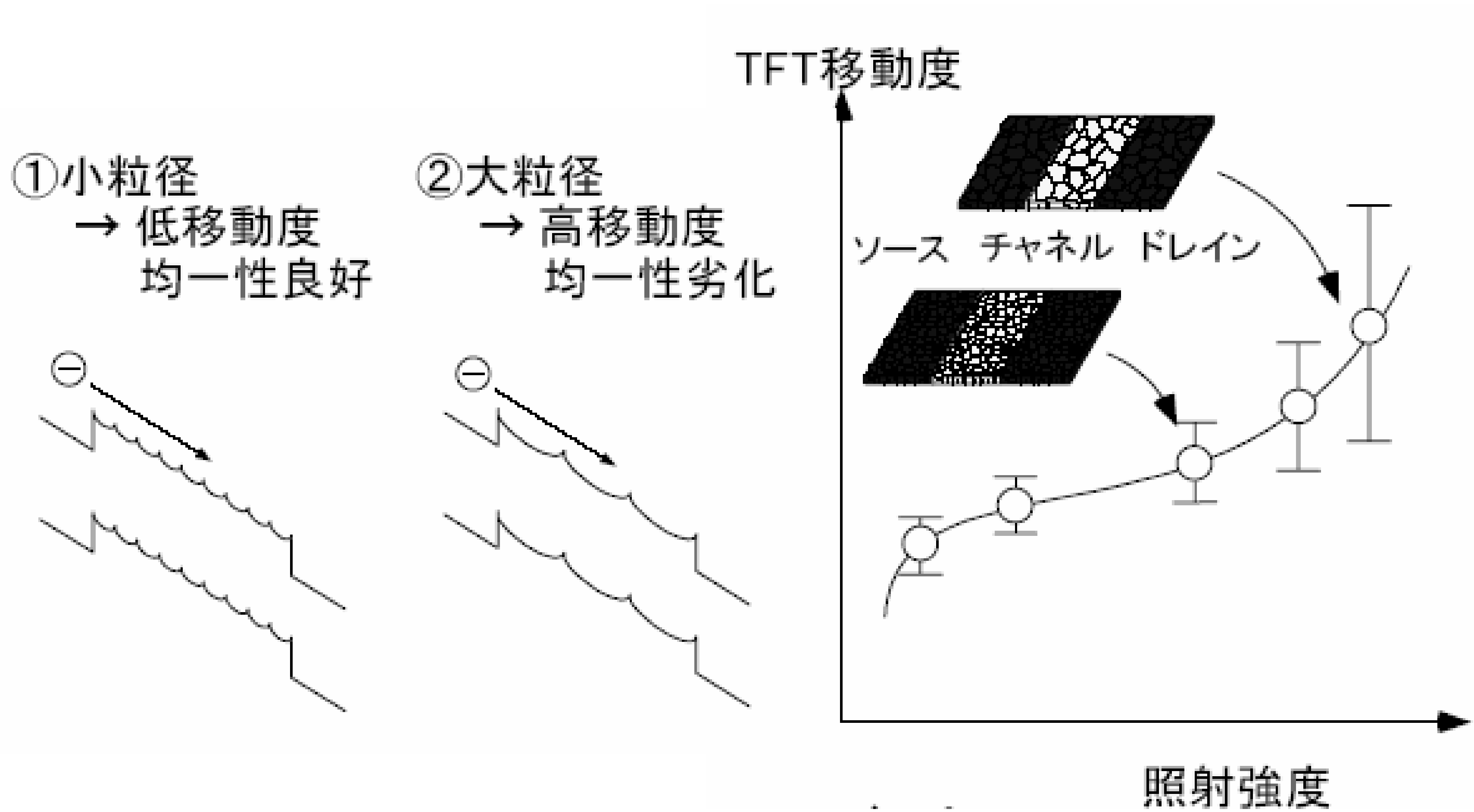
能量密度 : $I_m \sim I_a$

1. 矽膜完全融化
2. 過冷卻
3. Homogeneous nucleation

# 矽膜表面Secco etching後之電子顯微鏡照片



# TFT之移動率及其均一性




移動率與均一性為Trade off, 第一代LTPS裡優先均一性

# 結晶粒徑增大技術開發

## Grain size enlargement

→ elongating the melt duration

*1) Increasing the substrate temperature*

1um/RT → 1.5um/500$^{o}$C (100nm, SLG disc grain)

X1.5

*2) Thickening the Si film thickness*

2.5um/90nm → 3.8um/181nm (RT, micro-Cz)

X1.52

*3) Elongating the pulse duration*

2.5um/56ns → 3.5um/200ns (RT, 90~100nm, micro-Cz)

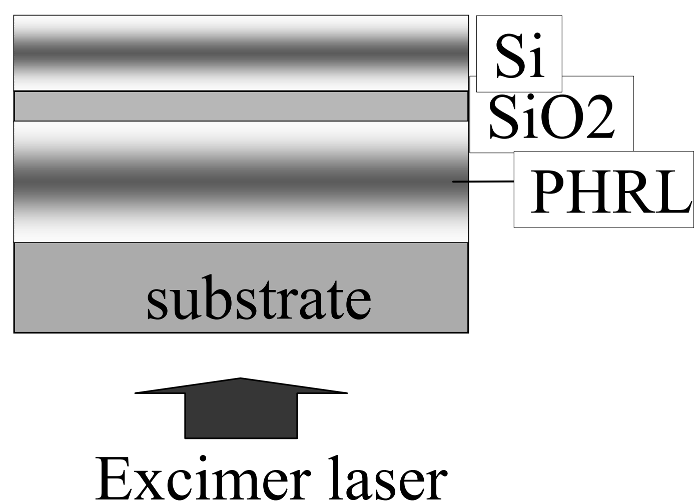
X1.4

Effects in above methods are limited!

**Our previous works**

Photosensitive (PHRL) as underlayer with laser from rear side

*W. Yeh, AMLCD 2002*



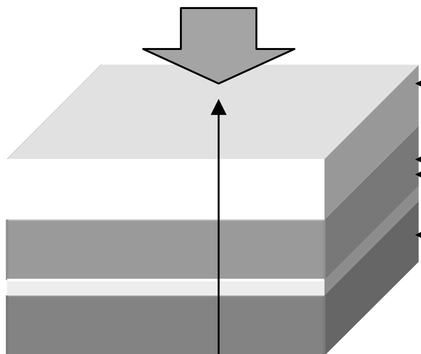

A part of laser energy was absorbed by the PHRL to rise its temperature during laser exposure

## Contents of this presentation:

1. PHRL underlayer enhanced grain growth
2. Melt duration measurement of Si film
   by time resolved optical measurement (TROM)
3. Novel grain location control method

# 1. PHRL underlayer enhanced grain growth

## Sample structure & preparation



**Substrate**

Corning glass, or quartz for KrF laser

**SiOxNy PHRL**

800nm, $\alpha$ =12K cm-1

SiH4 or Si(CH3)4 based PECVD @350 $^{o}$C

**Buffer SiO2 film**

100nm, PECVD the same as PHRL

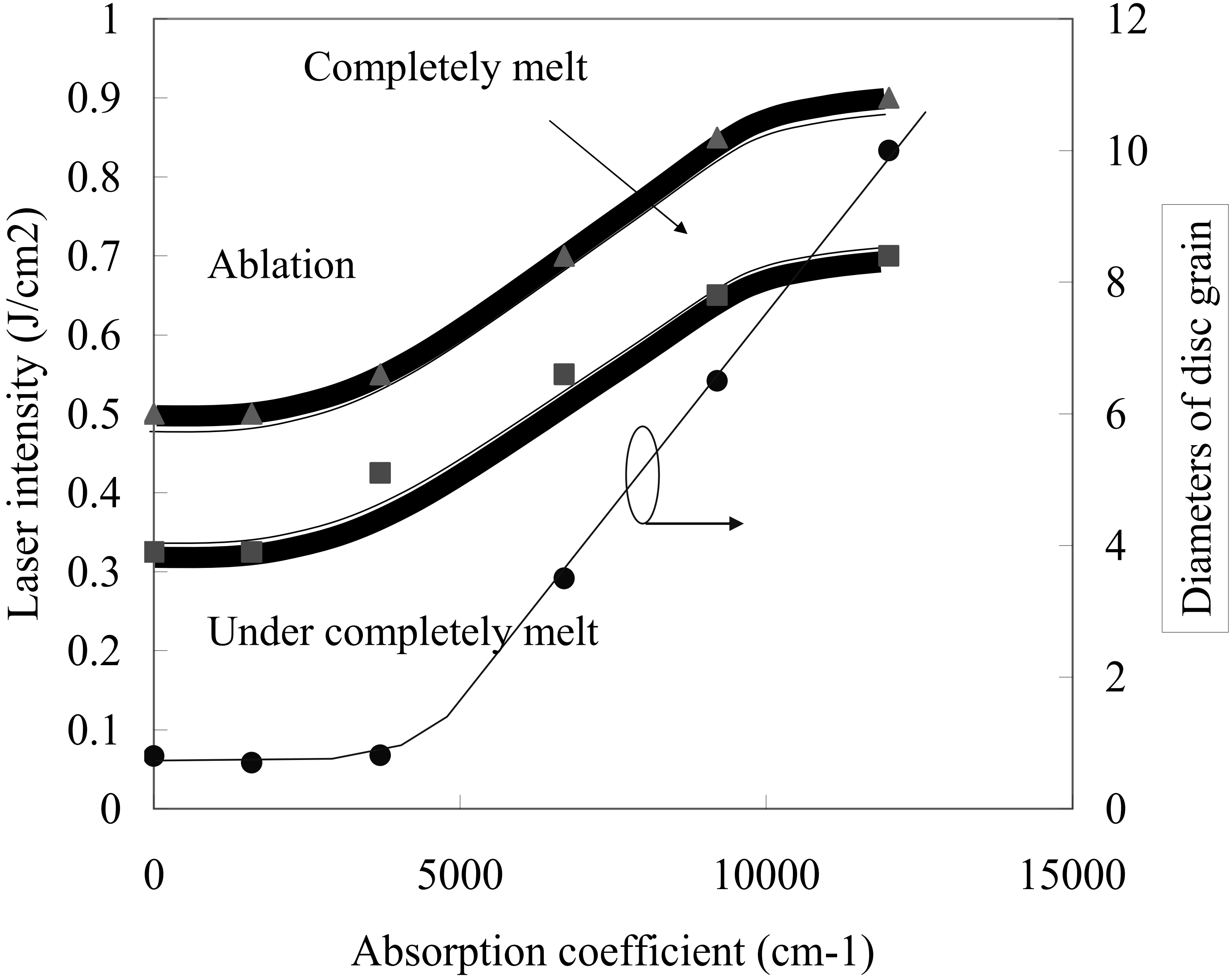
**a-Si film**

90nm, DC sputtering @200$^{o}$C

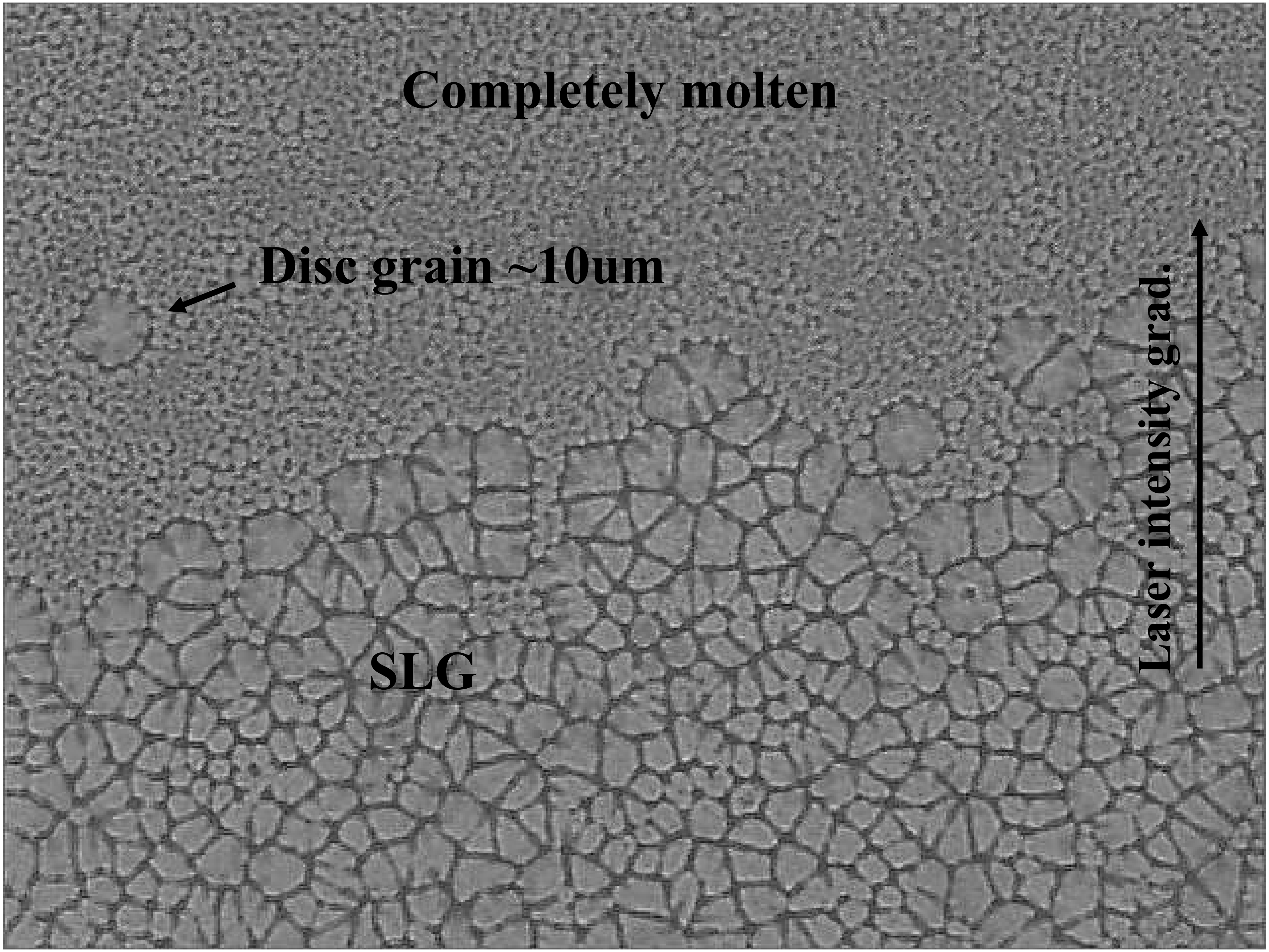
**ELA condition**

KrF or XeF, FWHM 25ns, 1pulse, RT

Critical laser intensity and grain size vs. $\alpha$



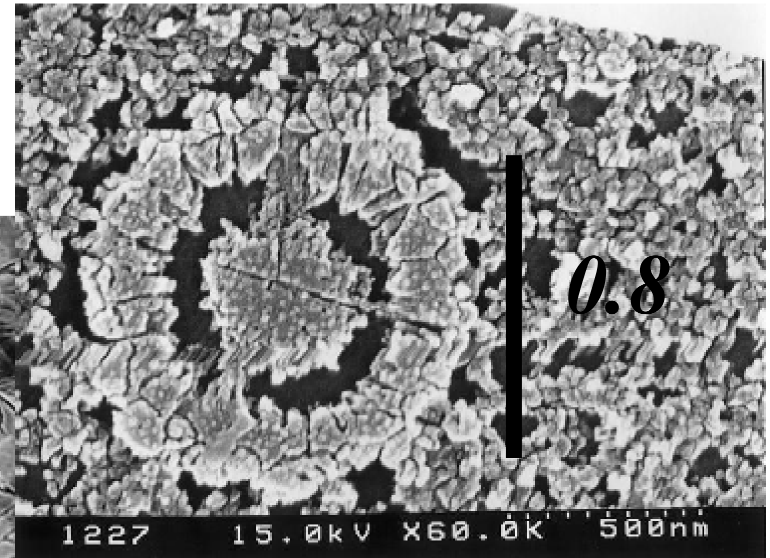
# permissive optical microscopy image



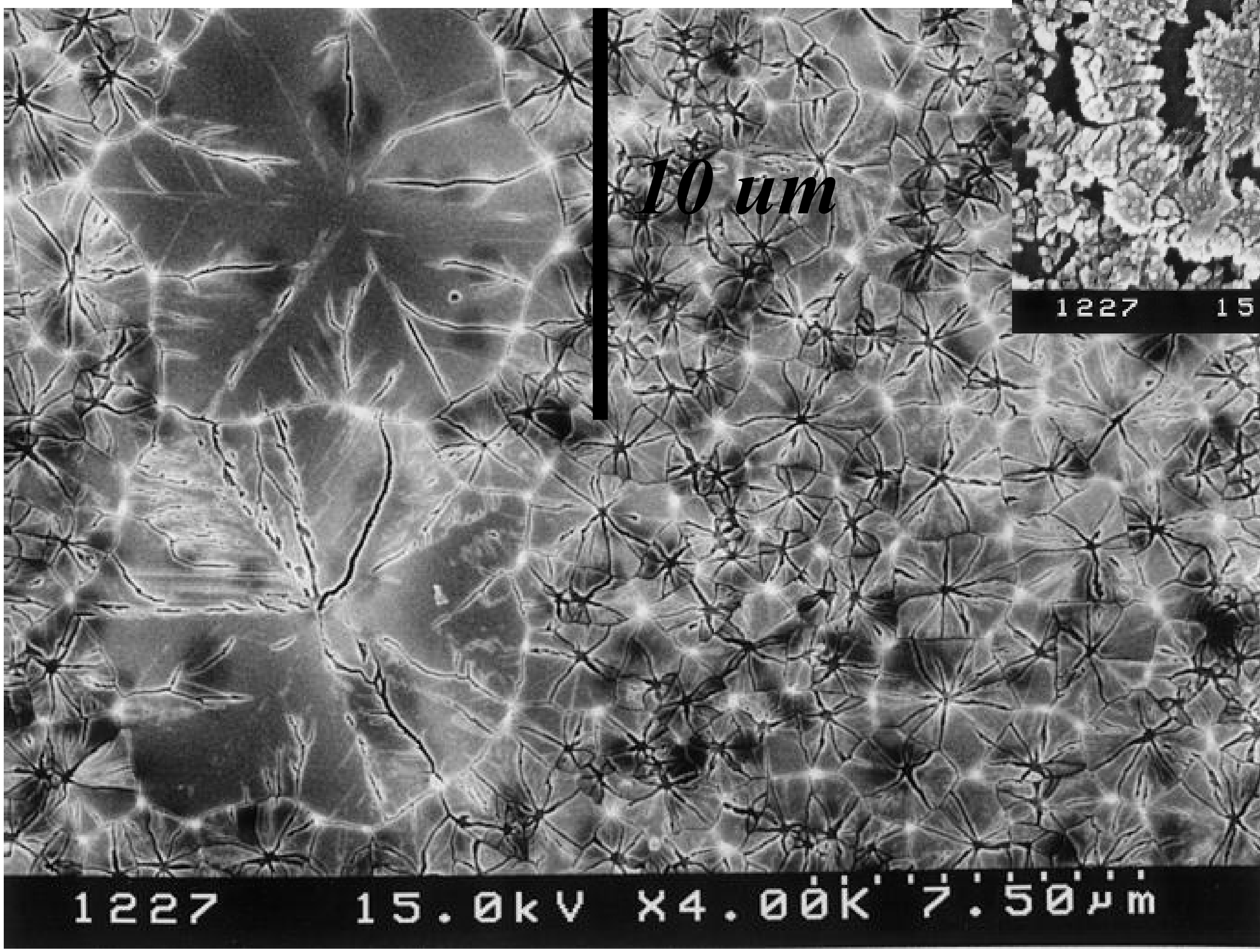
## Disc grain (SEM image after Secco-etch )

*W. Yeh, AMLCD 2002*

**100nm Si, RT**




Without PHRL

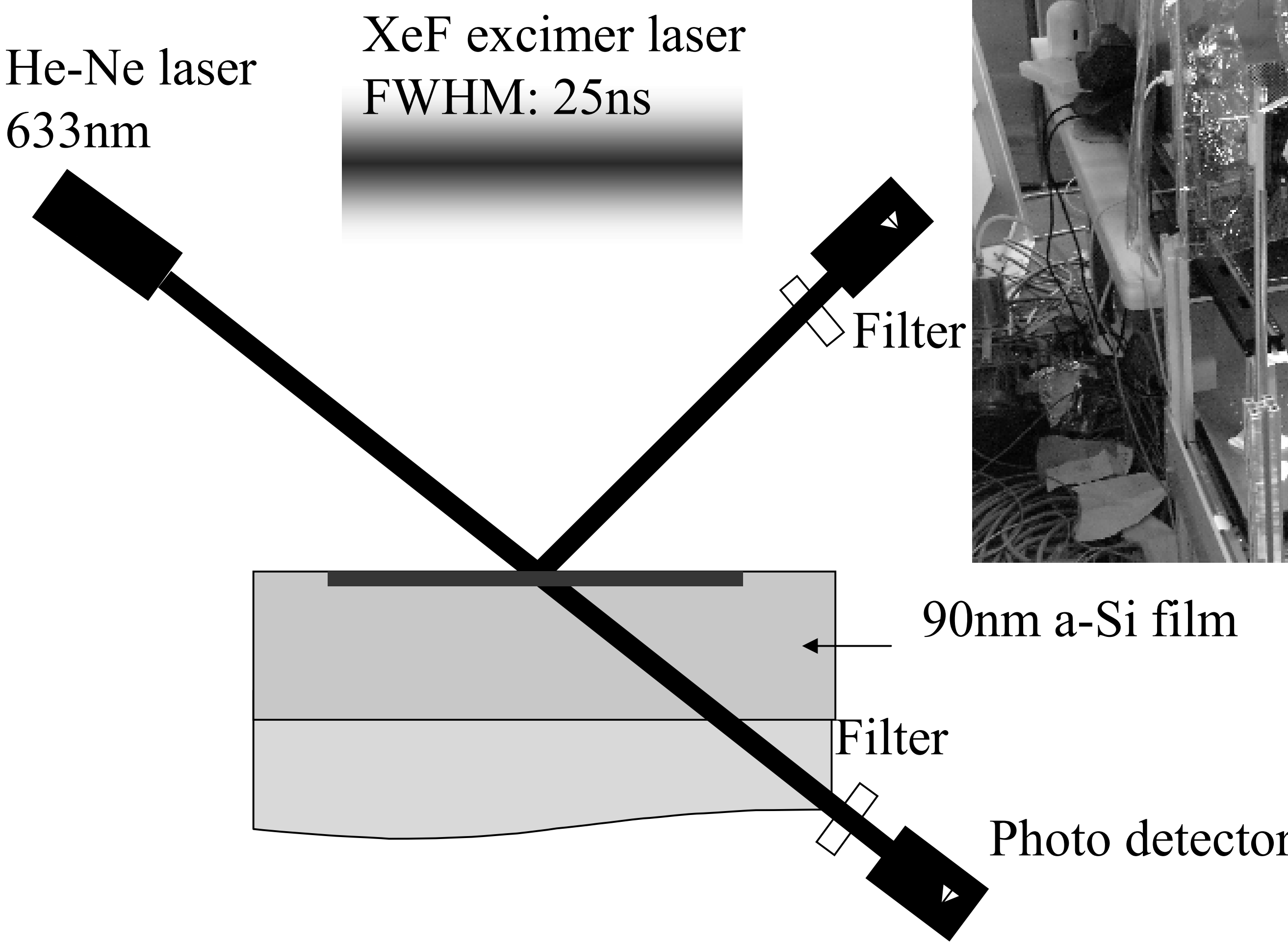


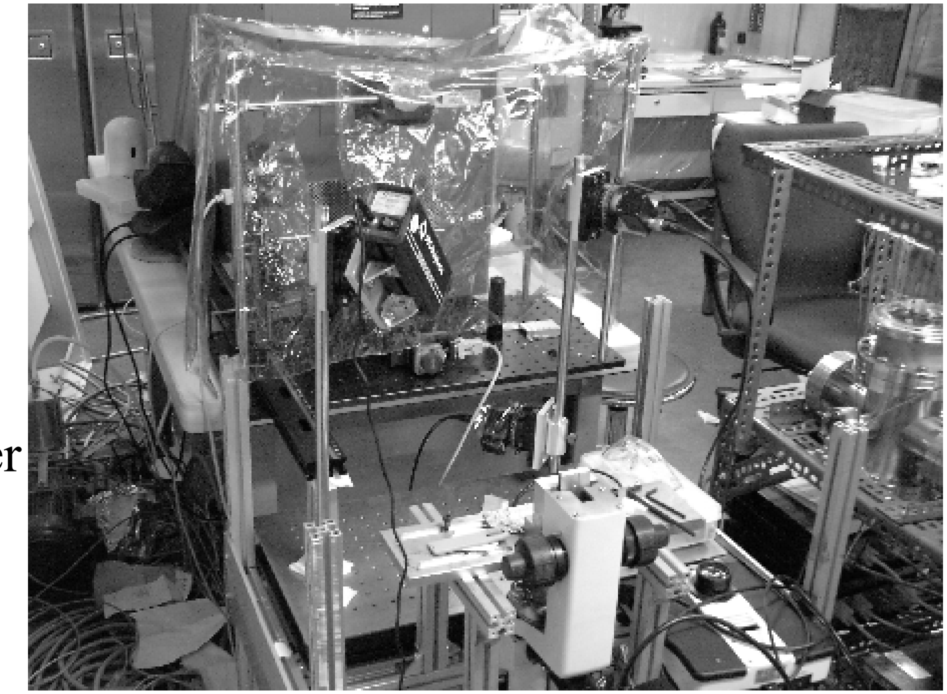

With PHRL, $\alpha = 12000 cm^{-1}$

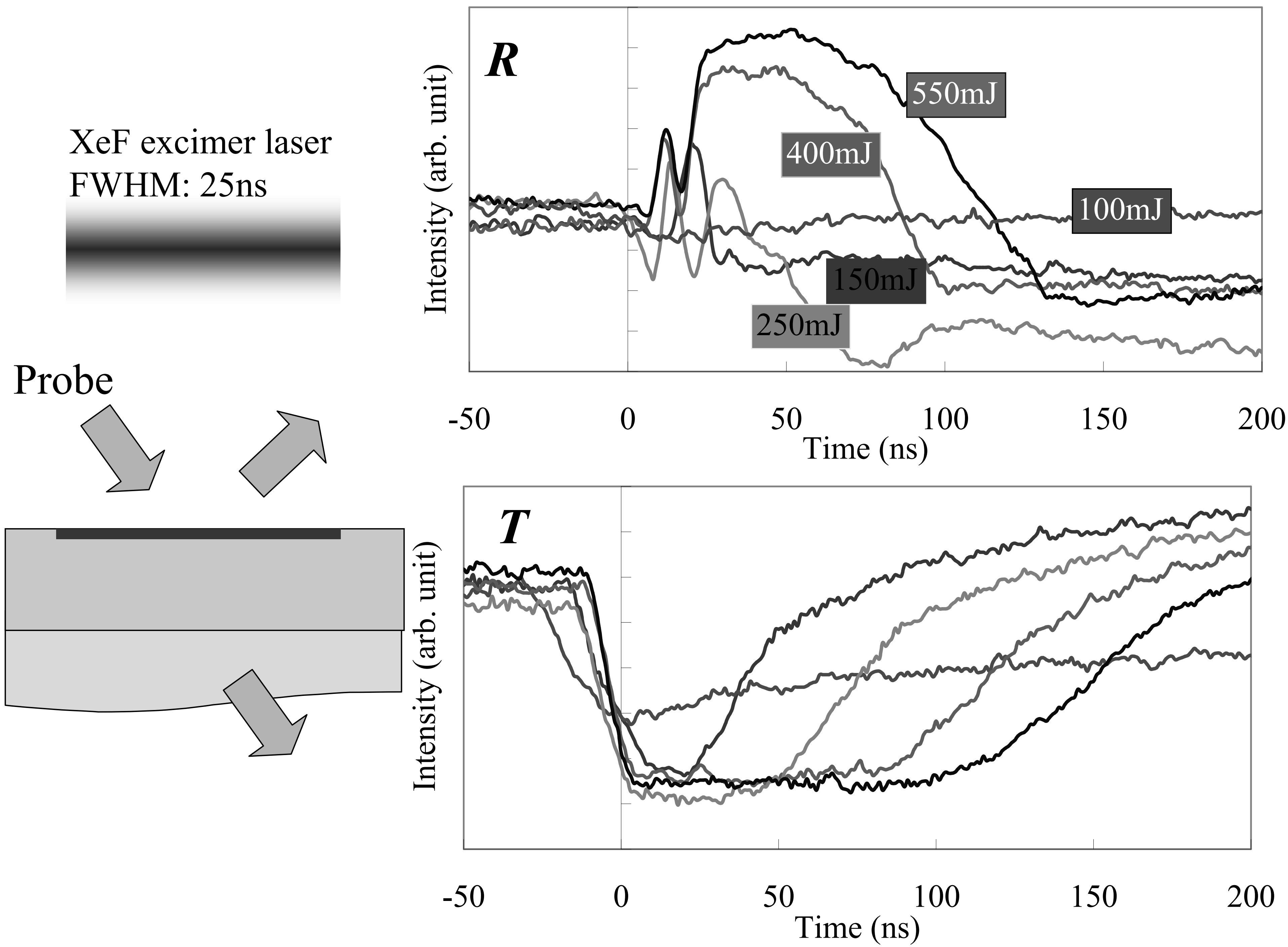
# 2. Time resolved optical measurement (TROM) system

台灣第一台, 由台科電子系葉文昌團隊及機械系鄭正元團隊合作製作

## Time-resolved optical system

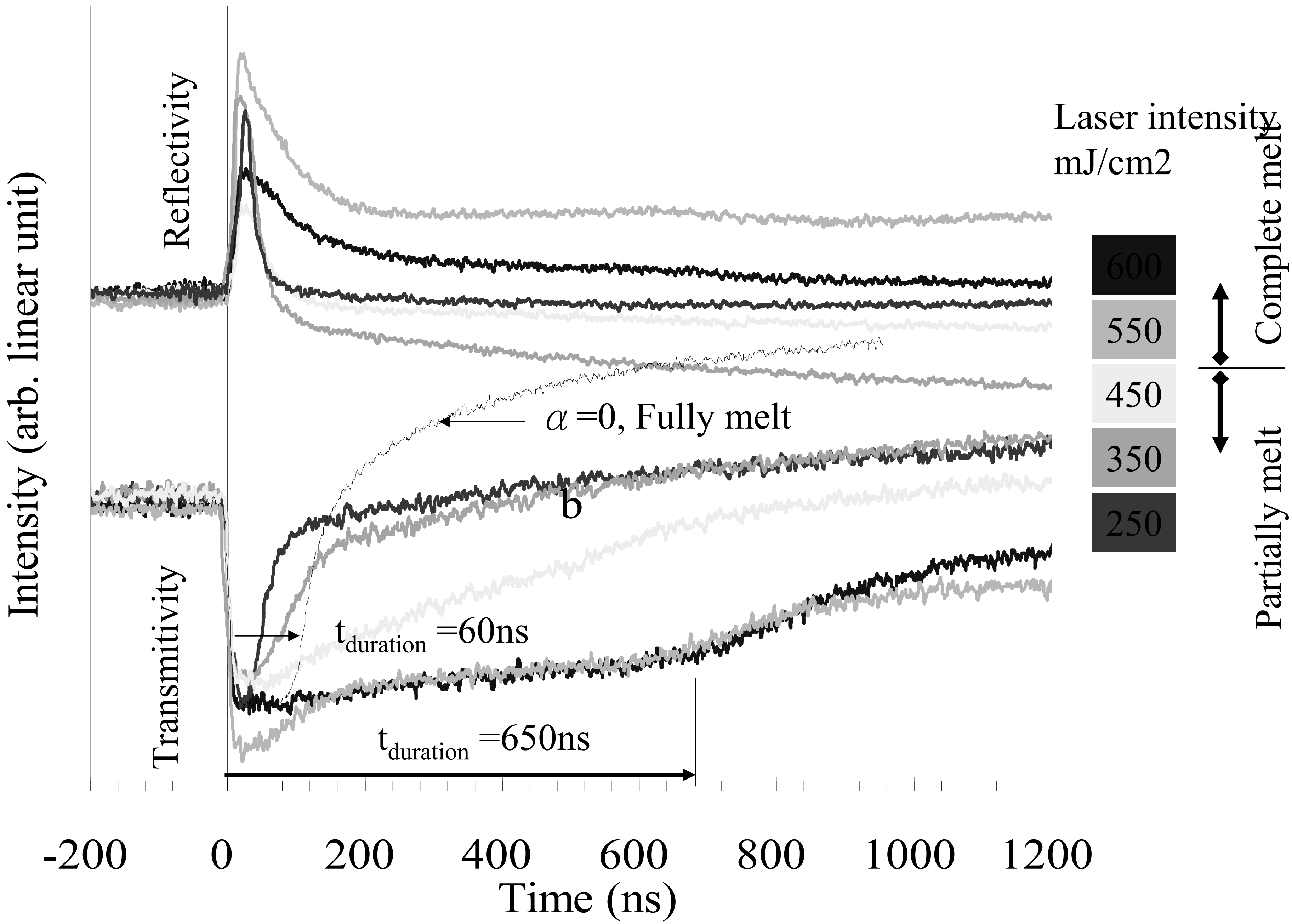




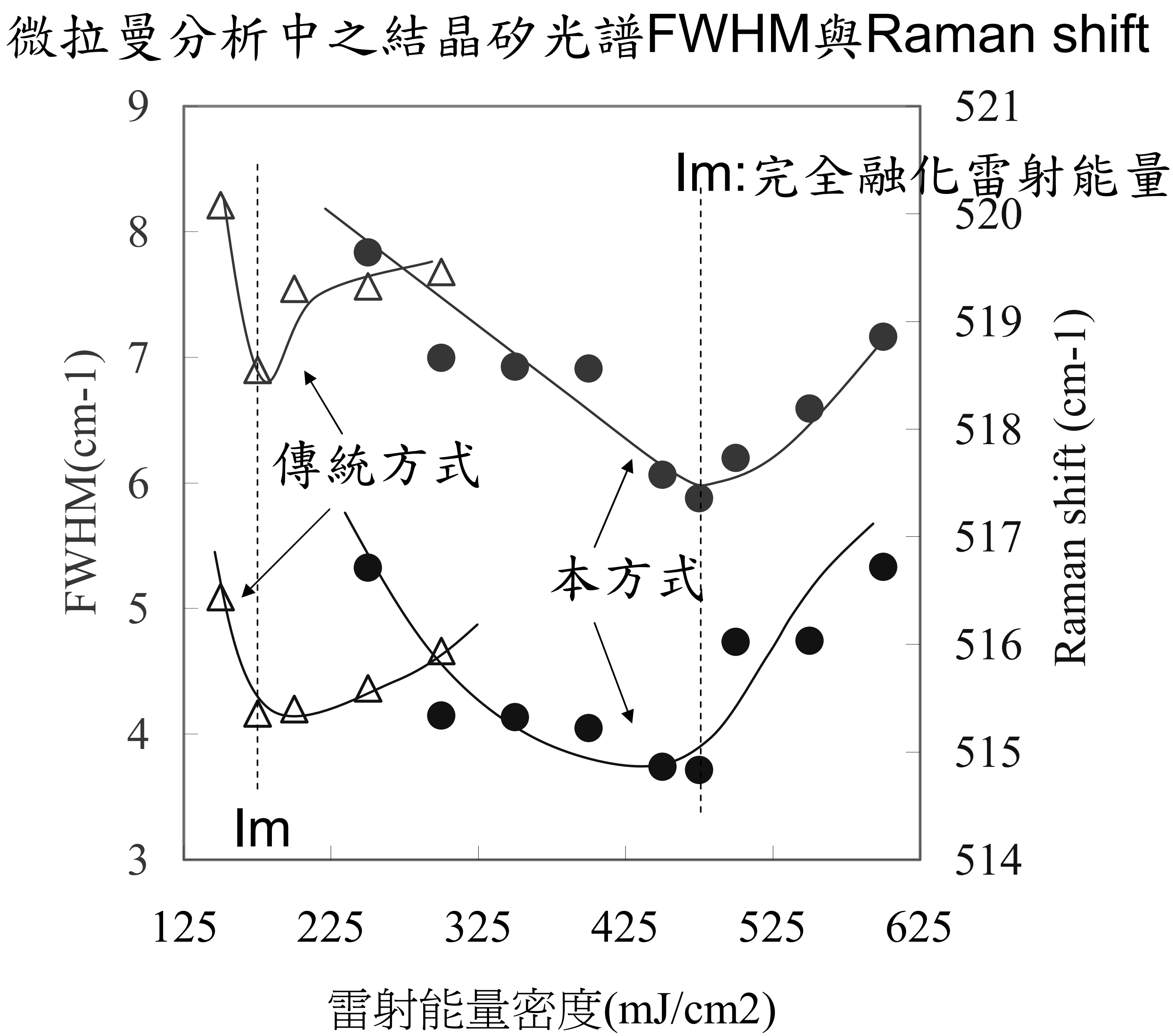
XeF excimer laser
FWHM: 25ns
Probe
R
550mJ
400mJ
100mJ
150mJ
250mJ
Intensity (arb. unit)
-50
0
50
100
150
200
Time (ns)
T
Intensity (arb. unit)
-50
0
50
100
150
200
Time (ns)

# HREC膜結構矽膜與傳統結構矽膜之TROM信號比較



→ HREC膜輔助結晶之矽膜融化時間為傳統結構矽膜之10倍,可說明結晶粒增大10倍之理由

# HREC膜結構矽膜與傳統結構矽膜之結晶性與膜中應力比較



本方式所得矽膜比傳統方式

FWHM: 6.9 → 4.3 cm-1

Raman shift 偏離量: 4.7 → 5.2 cm-1

表示結晶性得到很大改善, 且膜中應力增加

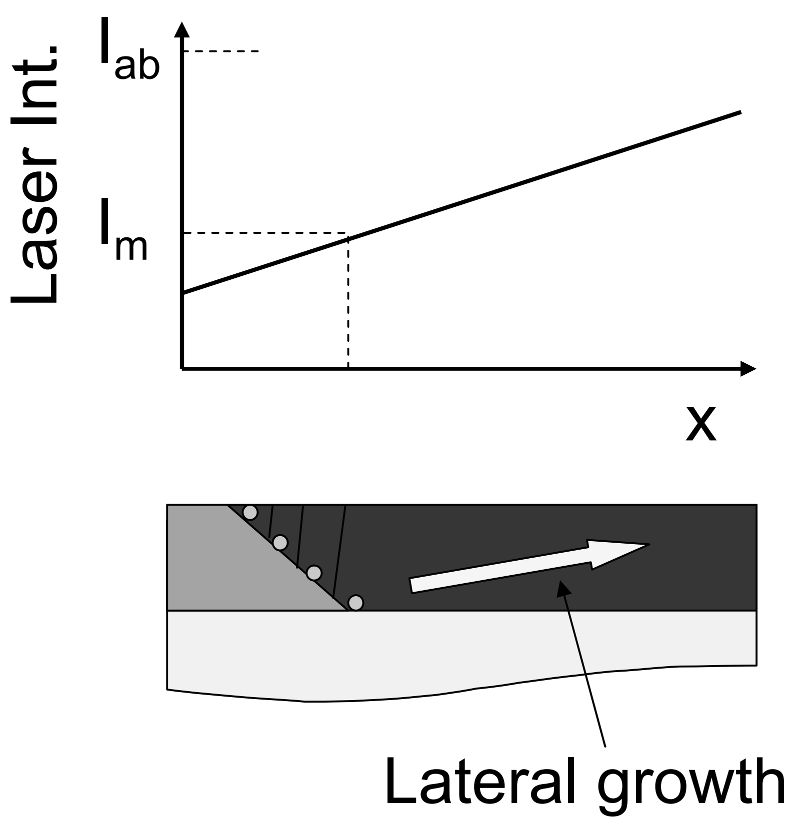
→ 有助於提高移動率及均一性

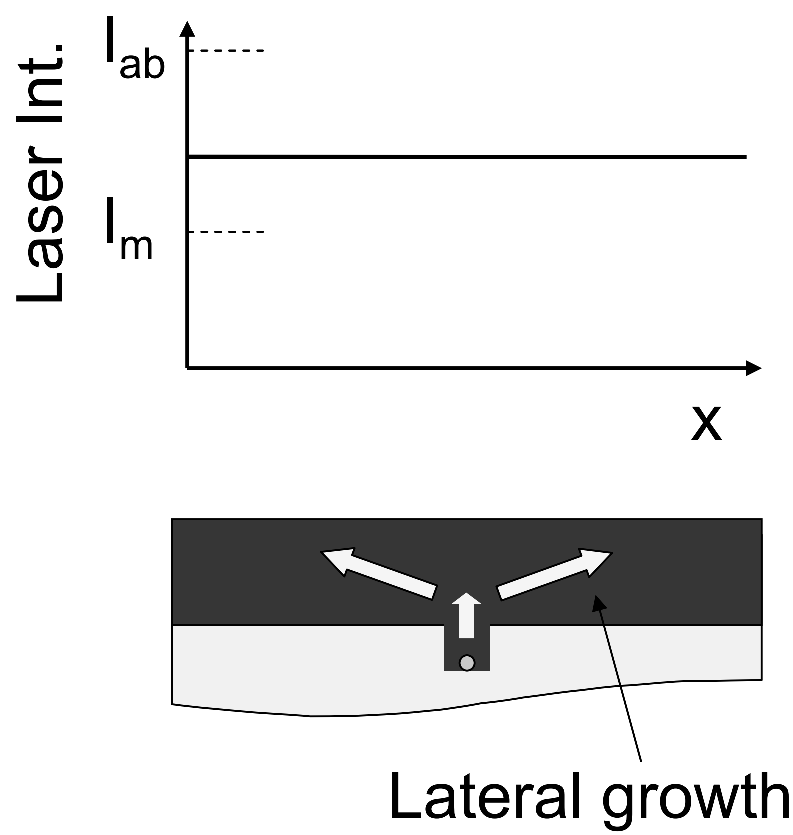
次世代LTPS

Lateral growth

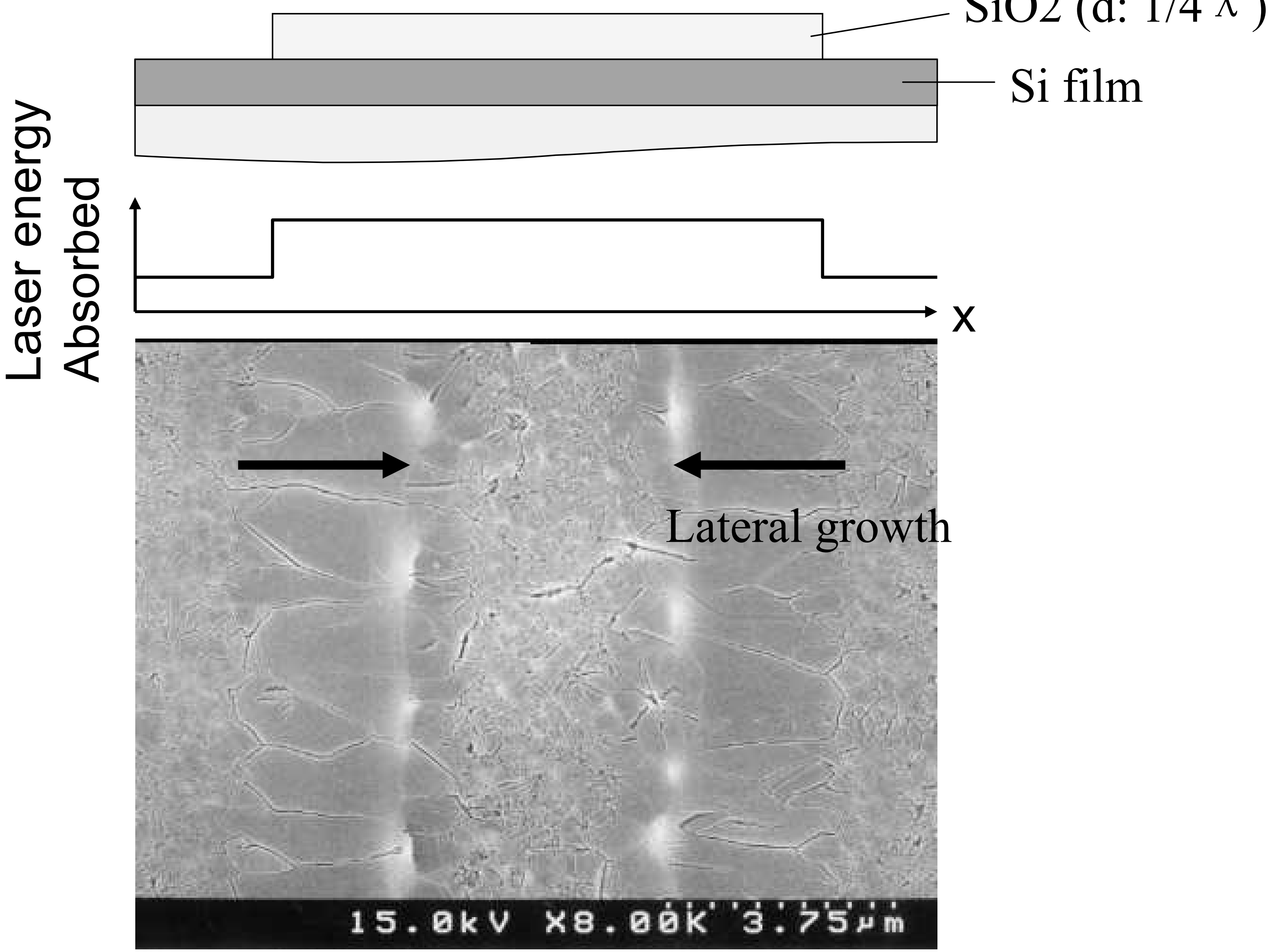
控制結晶核發生位置

Ex. 改變雷射光強度分佈, 矽膜厚度分佈…



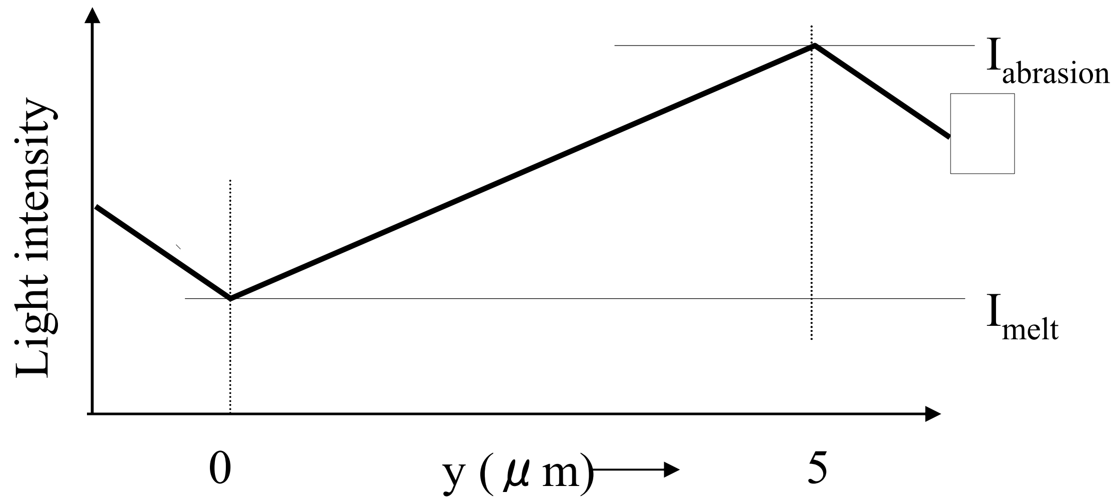



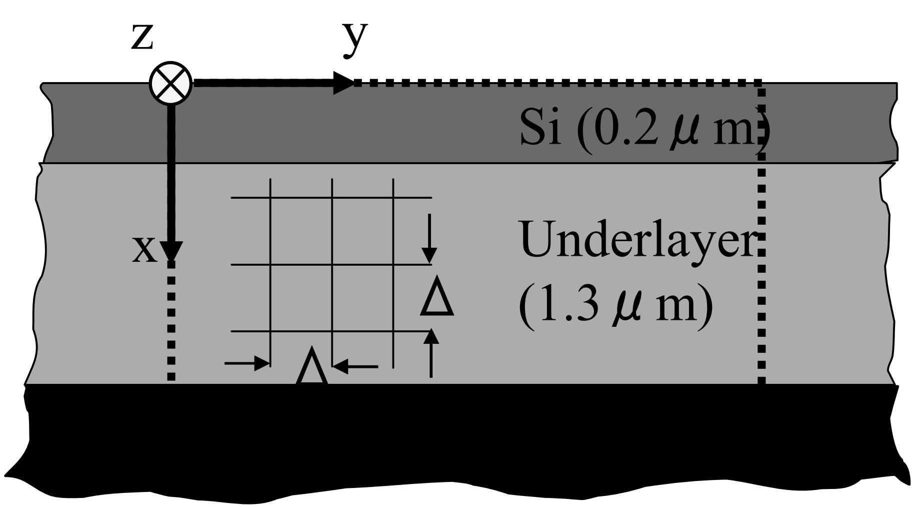
# Super lateral growth (1996 by J.Im, Columbia Univ.



# 準分子雷射誘發橫向長晶之數值模擬

## 計算模式




$$c\frac{\partial T}{\partial t} = \nabla \cdot (\kappa \nabla T) + S_1 - \frac{\partial}{\partial t} S_2$$

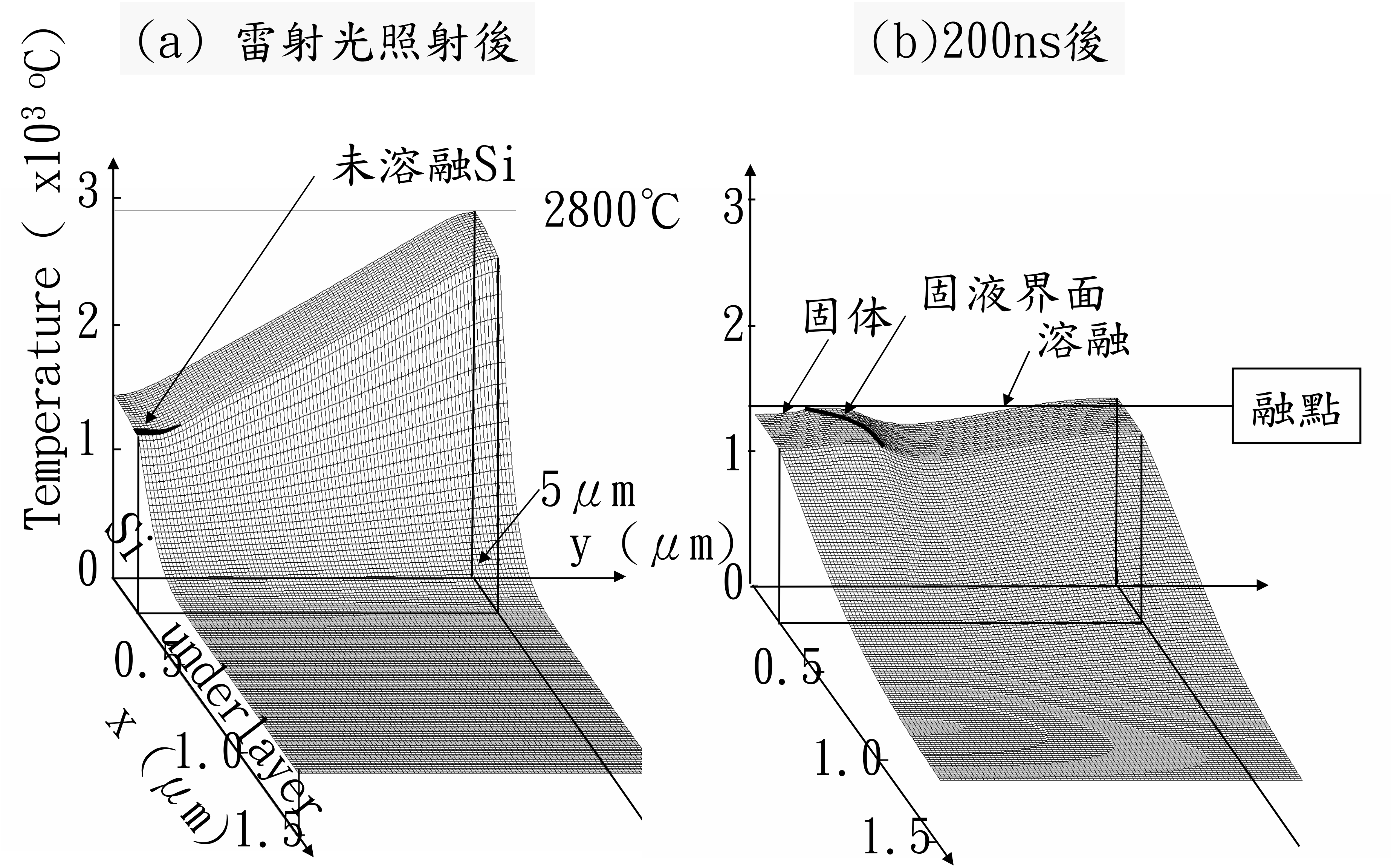
c ：熱容量

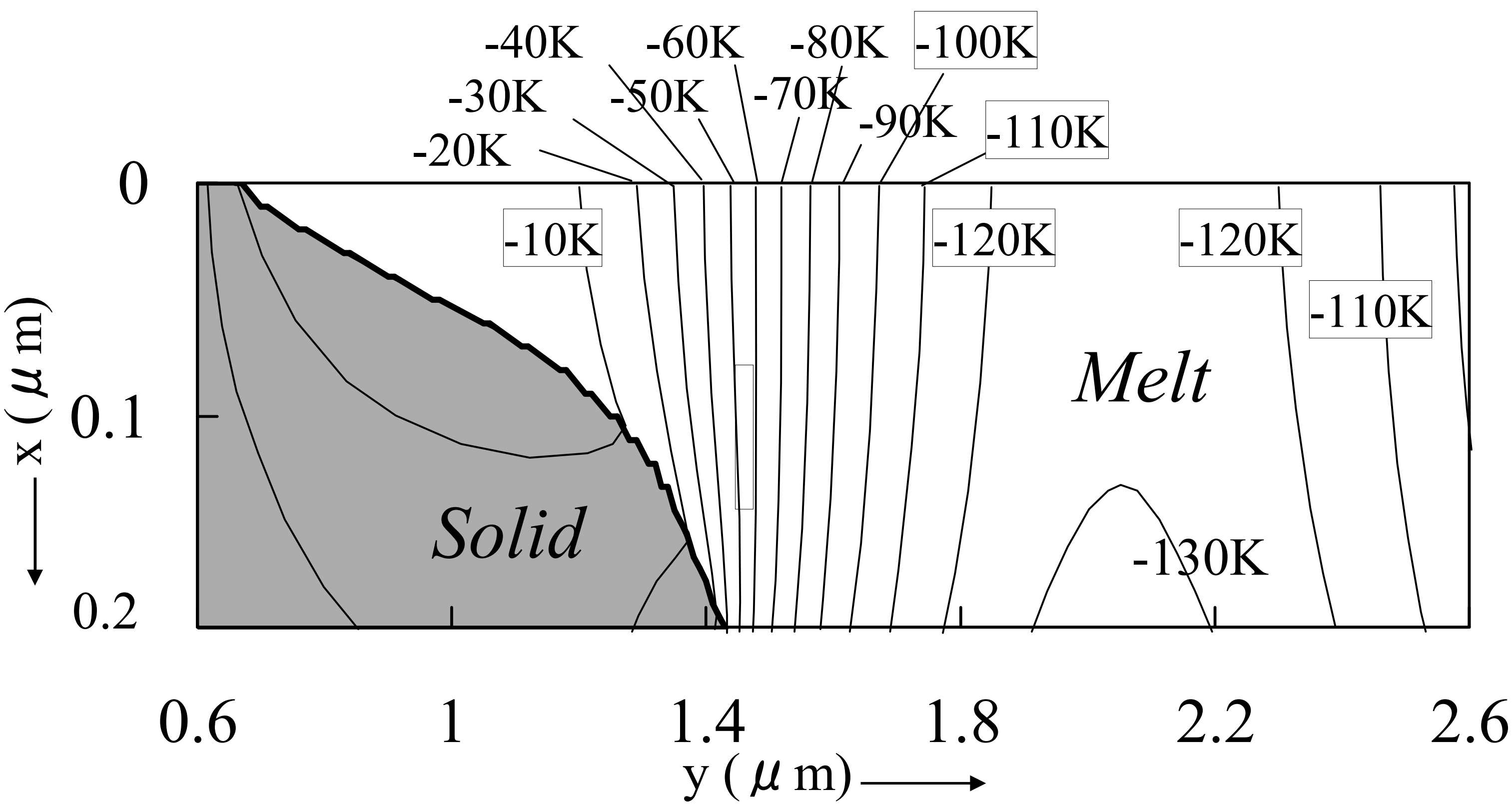
$\kappa$ ：熱傳導率

$S_1$：吸放熱速度

$S_2$：潛熱之蓄積密度

# 膜内溫度分布之時間依存性





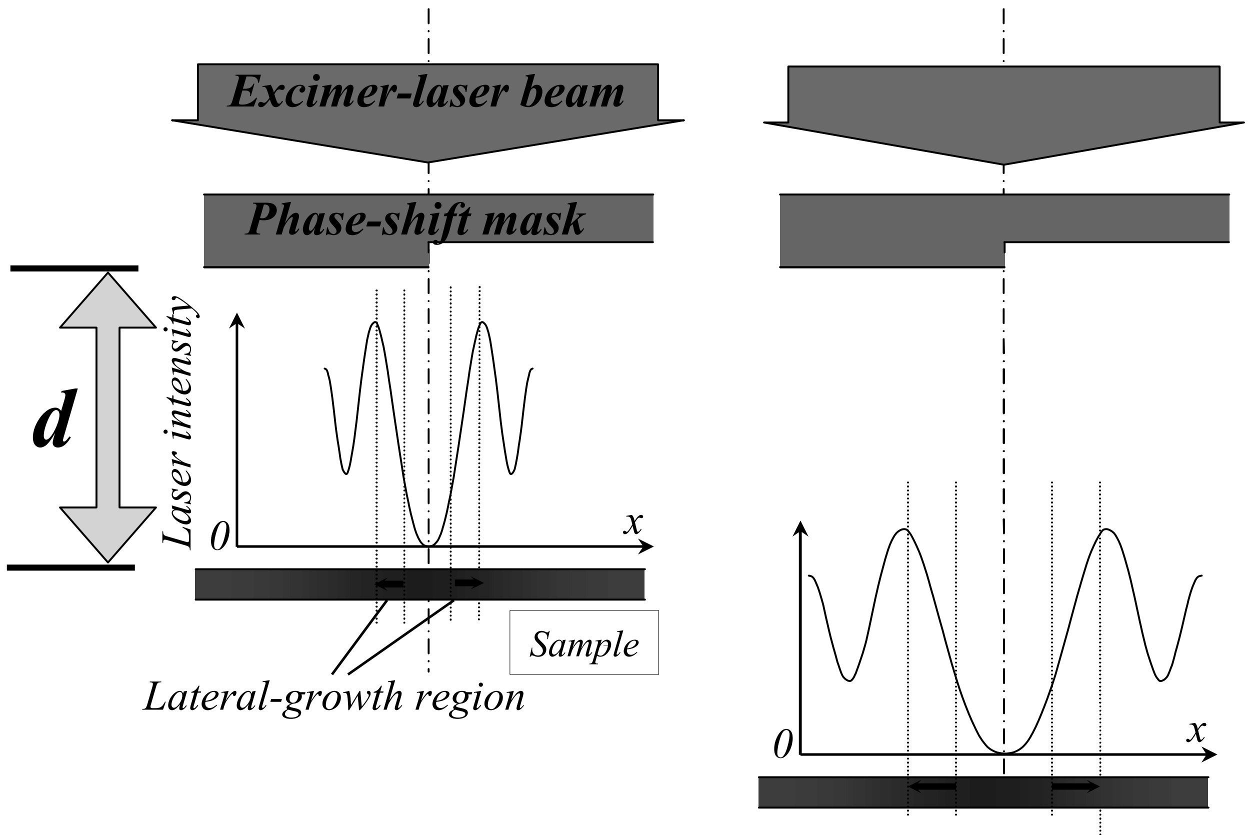

結晶前方存在強過冷卻之區域 → 結晶核在此發生

# 橫向長晶技術開發

# SLS (Sequential lateral solidification)

# Phase-modulated excimer-laser annealing (PMELA)

*(C.Oh et. al.,1998)*




Energy gradient can be modulated by adjusting the mask-sample distance d

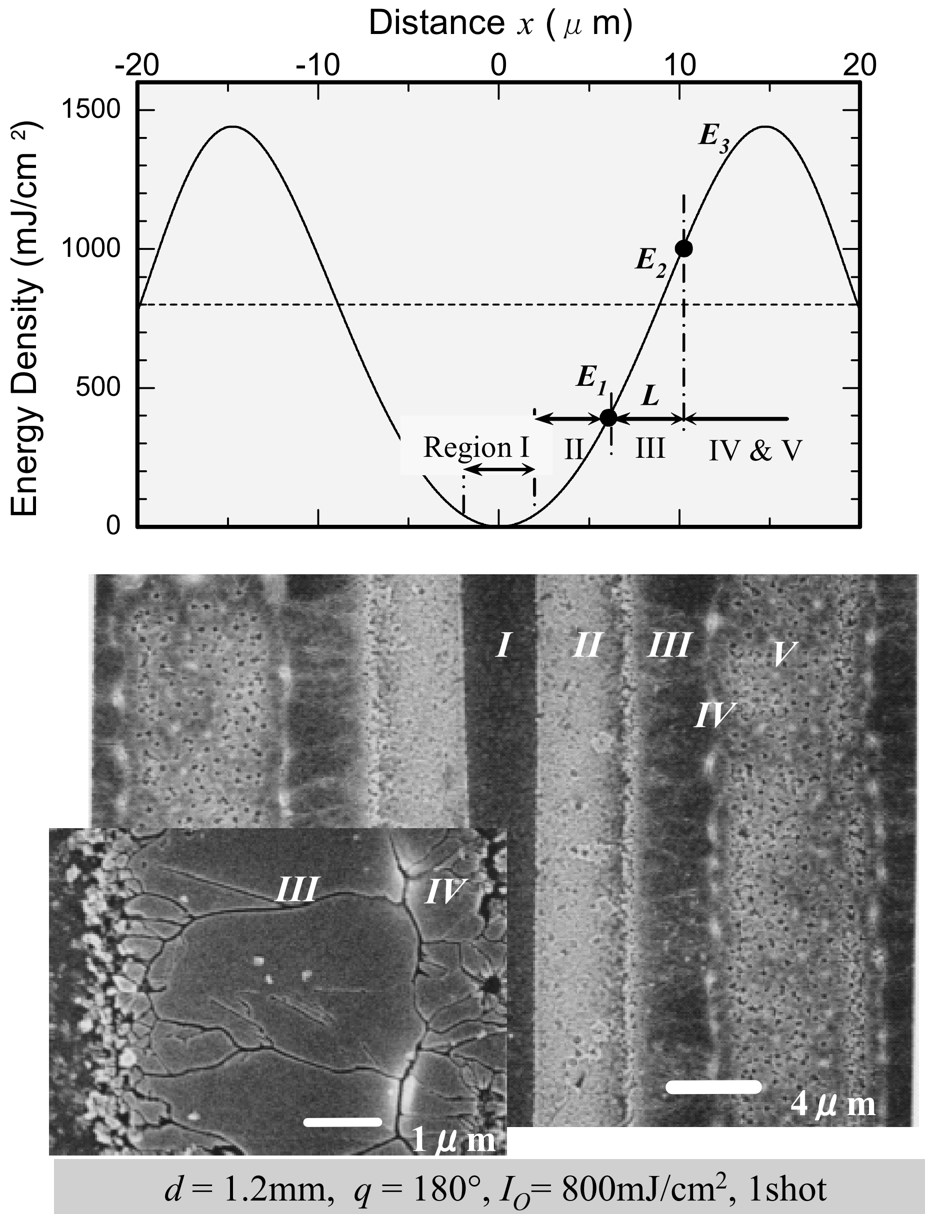



Fig. 1.10 SEM photograph of the film crystalllinzed by the linear phase-shift mask with q = 180$^o$

# Micro-CZ法 (Ishihara et al,. 2000, Delft Univ.)

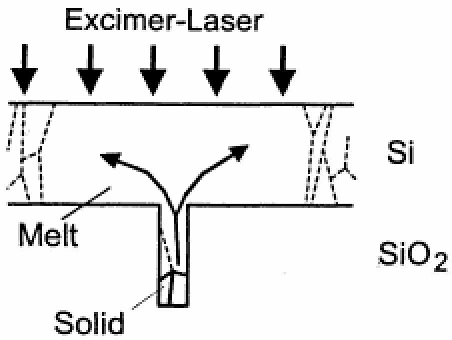



Figure 1: Schematic viewgraph of $\mu$-Czochralski (grain-filter) process

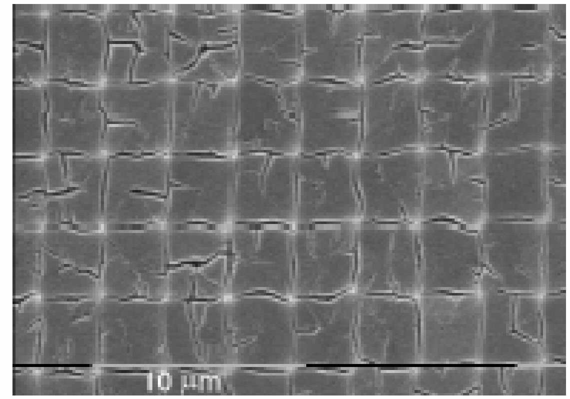
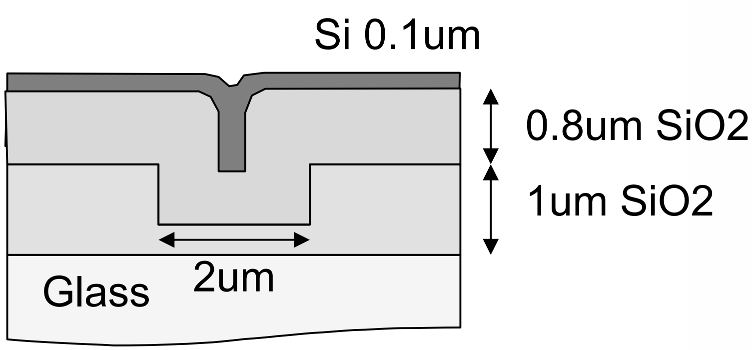



Figure1. SEM image of Si film after laser crystallization



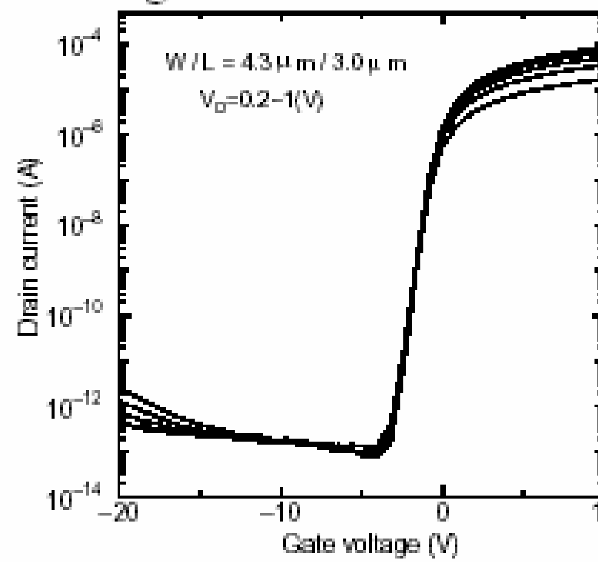




Figure 2. Transfer characteristics of c-Si TFTs

2D locating of grain had achieved for the first time

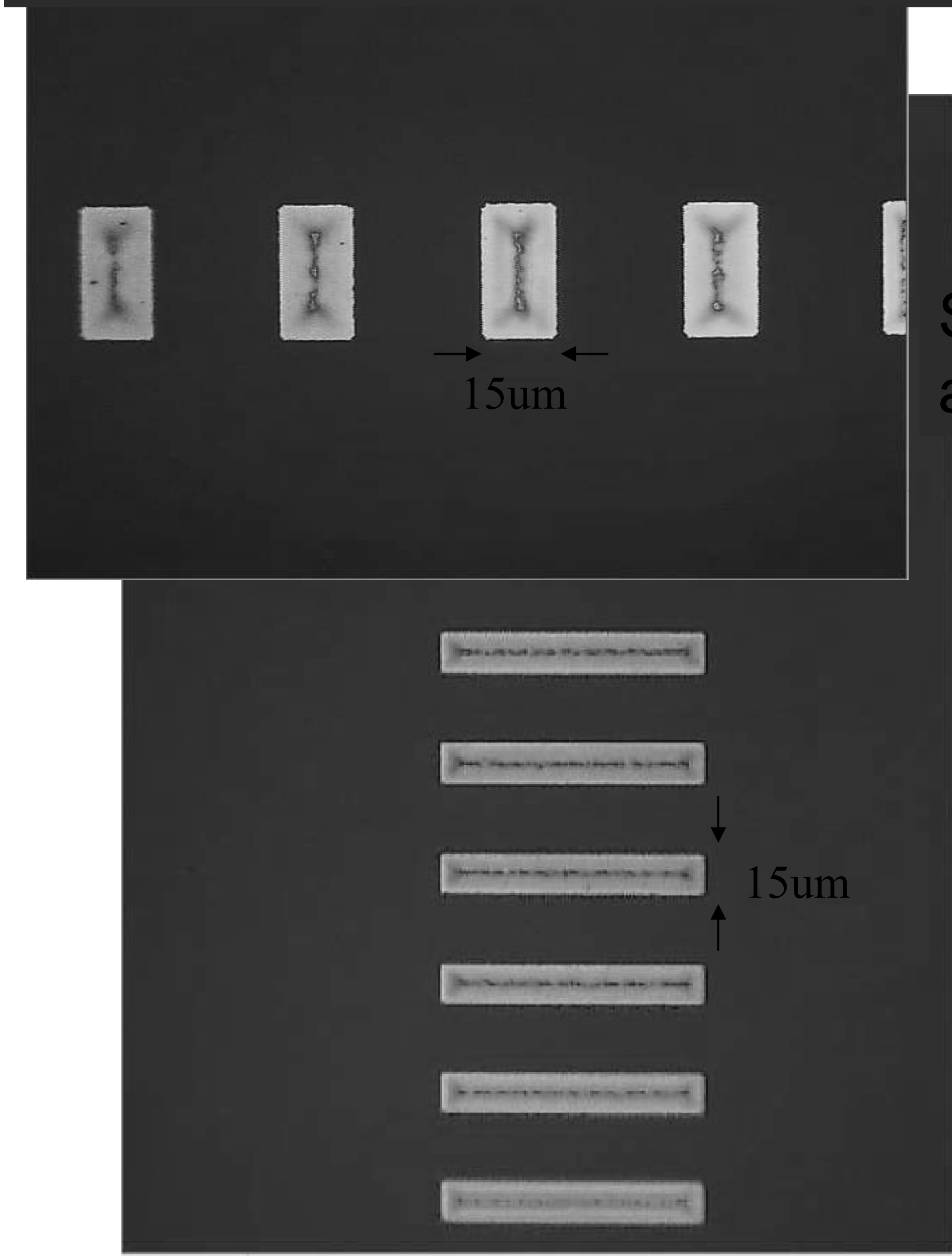
## 本實驗室原創手法: HREC法, 2002


(a) Cross sectional view

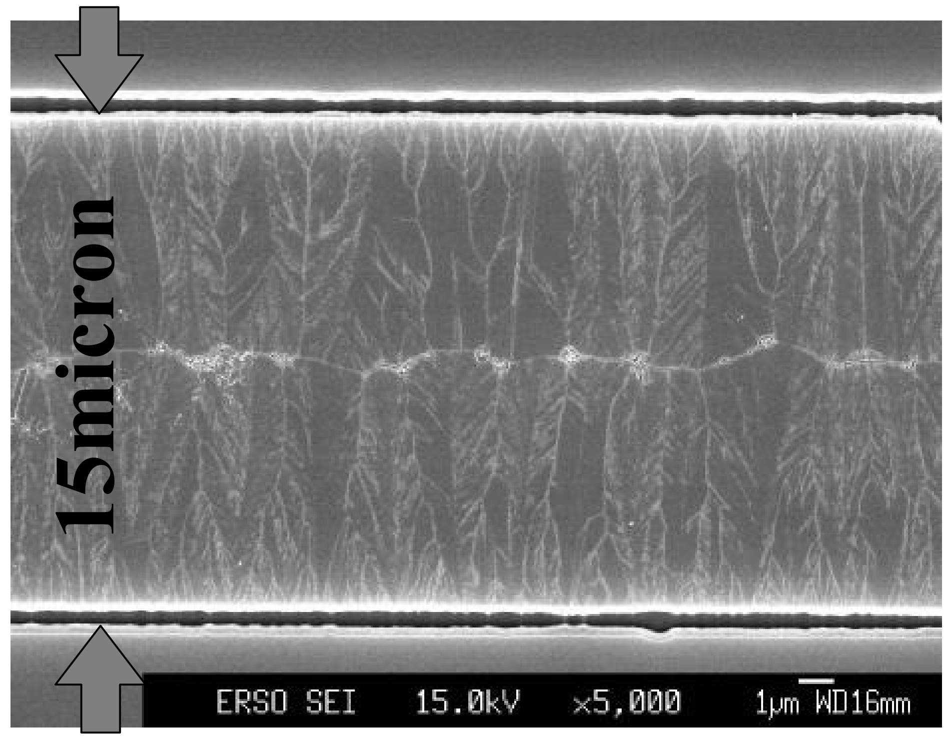
(b) Overlook view of Si island

(c) Proposed TFT structure

# Optical images of HREC Si islands



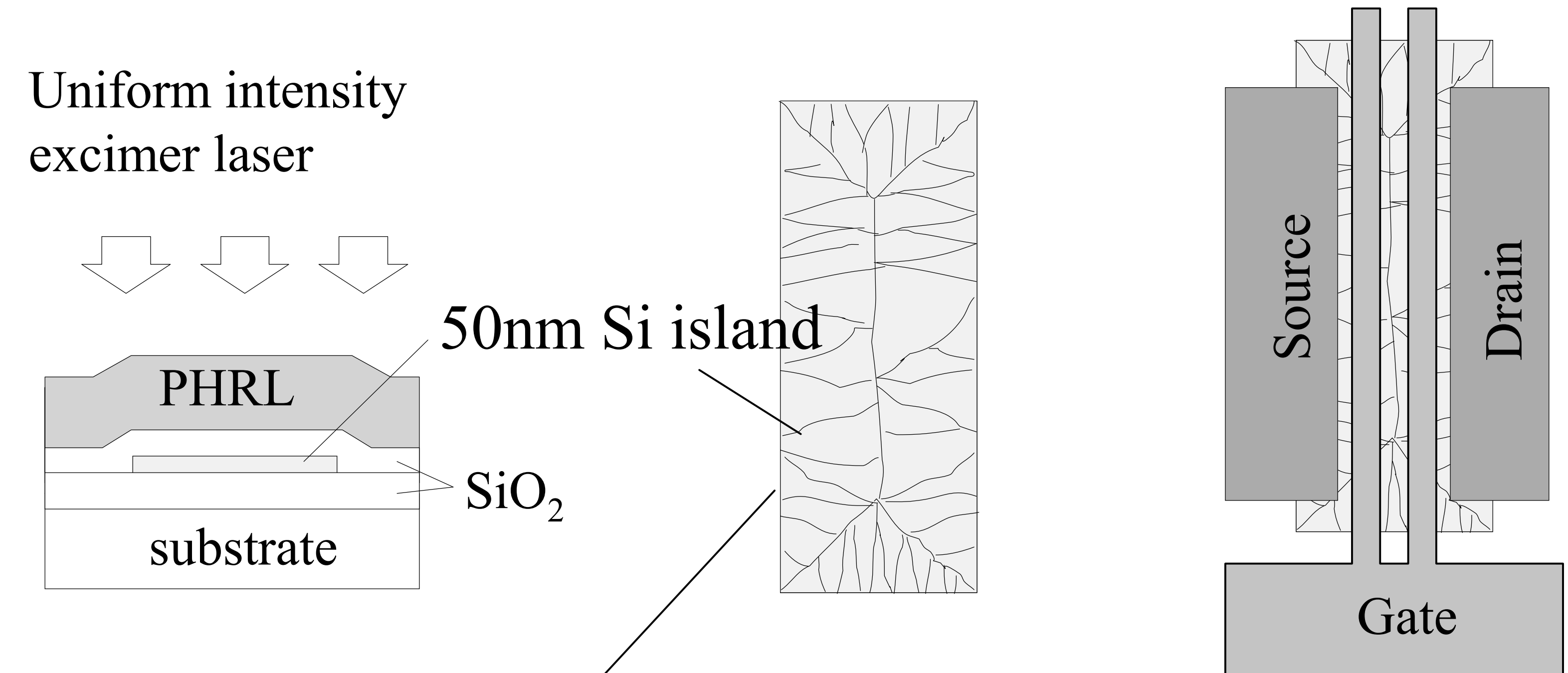

# SEM images of HREC Si islands after Secco etching



## 3. Location control of lateral grain with PHRL

## [redacted]

*W. Yeh et. al. AMLCD2003*




(a) Cross sectional view

(b) Overlook view of Si island

(c) Proposed TFT structure

Nucleation take place spontaneously from the edge of island

# Comparison of laser-induced lateral growth methods

| | New laser system | Alinment. to X'tal | Addition. photolitho. processes |
|---|---|---|---|
| SLS | V | V | |
| PMELA | V | V | |
| Micro-Cz | | V | V |
| **HREC** | | | |

# 次世代絕緣膜技術開發

改善要點:

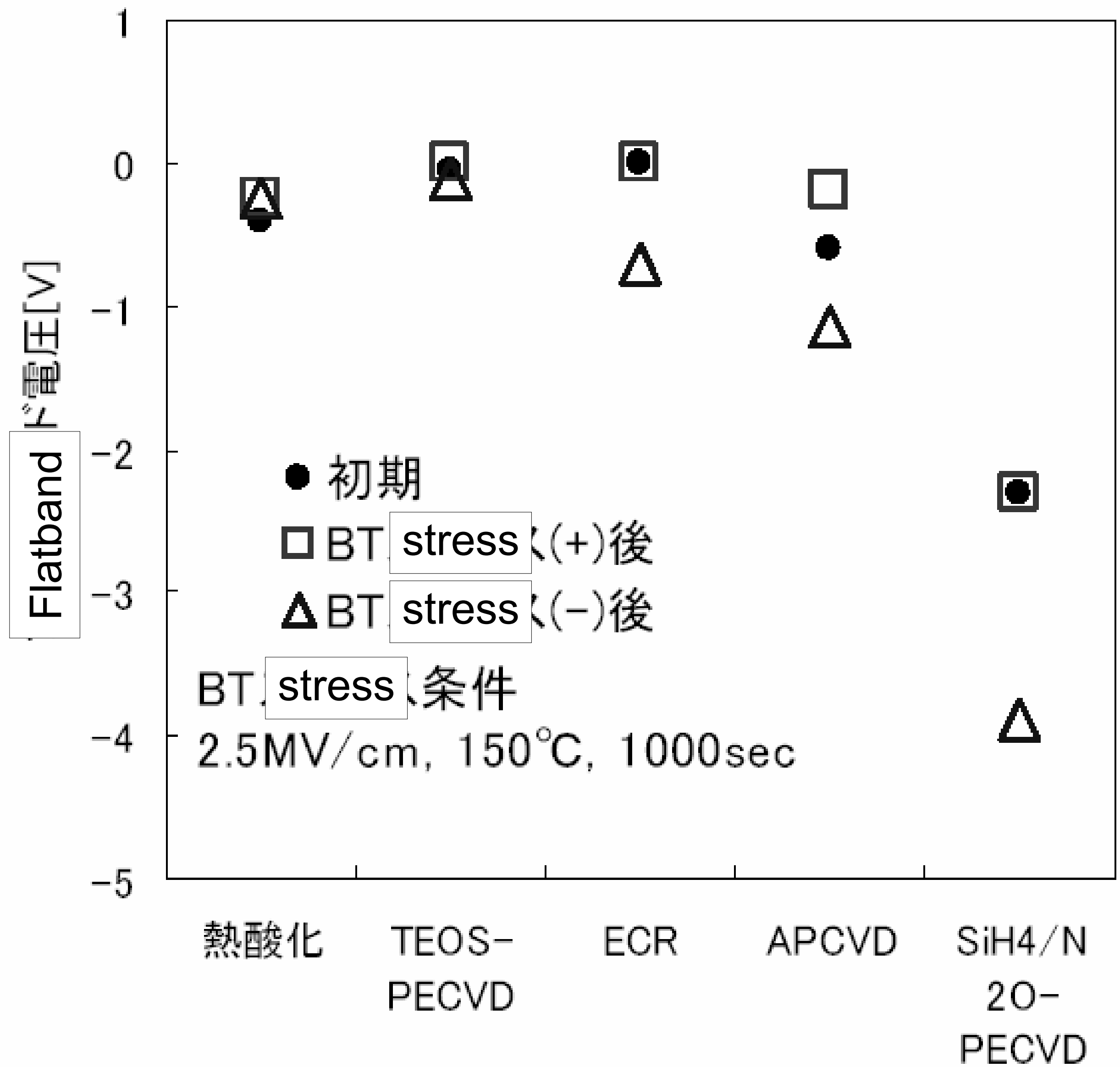
1. 膜中電荷 (cm-2)
2. SiO2/Si界面陷井密度(cm-2ev-1)
3. 阻值
4. 崩潰電場(E)
5. 介電係數

電性探討:

MOS二極結構之IV, CV特性量測

物性探討: Ex. SiO2

| | | |
|---|---|---|
| Ellipsometers | 光學常數 | n值 |
| FTIR | 膜中鍵結 | Si-O, Si-H, -OH, Si-C… |
| XPS | 原子結合狀況 | Si-O, Si-O2, Si-O3, Si-O4 |
| AES | 原子比值 | Si:O:N:C:H = ?, etc. |




N. Ibaraki, SID 99 Digest, pp.172-175, 1999.

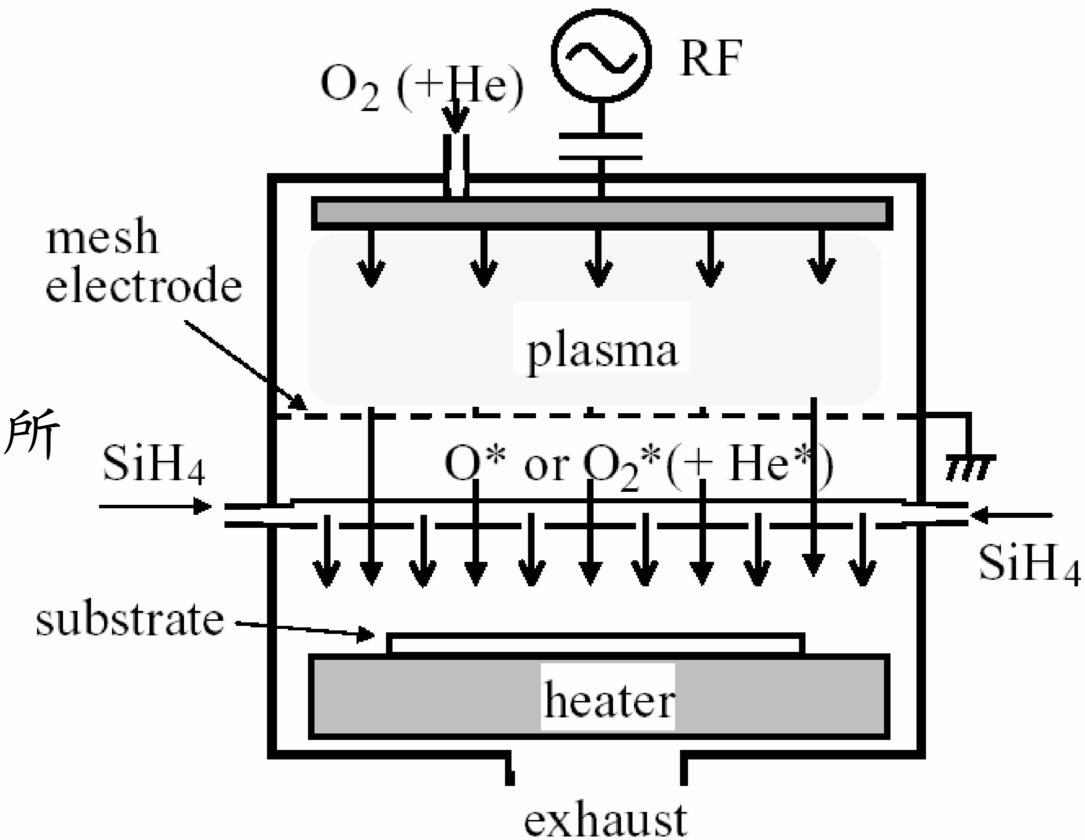
# 其他目前開發中之良質絕緣膜沉積技術

## Remote PECVD (NEC)

將電漿發生區域
與基板分離

↓

減少電漿高能離子所
造成之損傷



# 光氧化+PECVD by Sharp

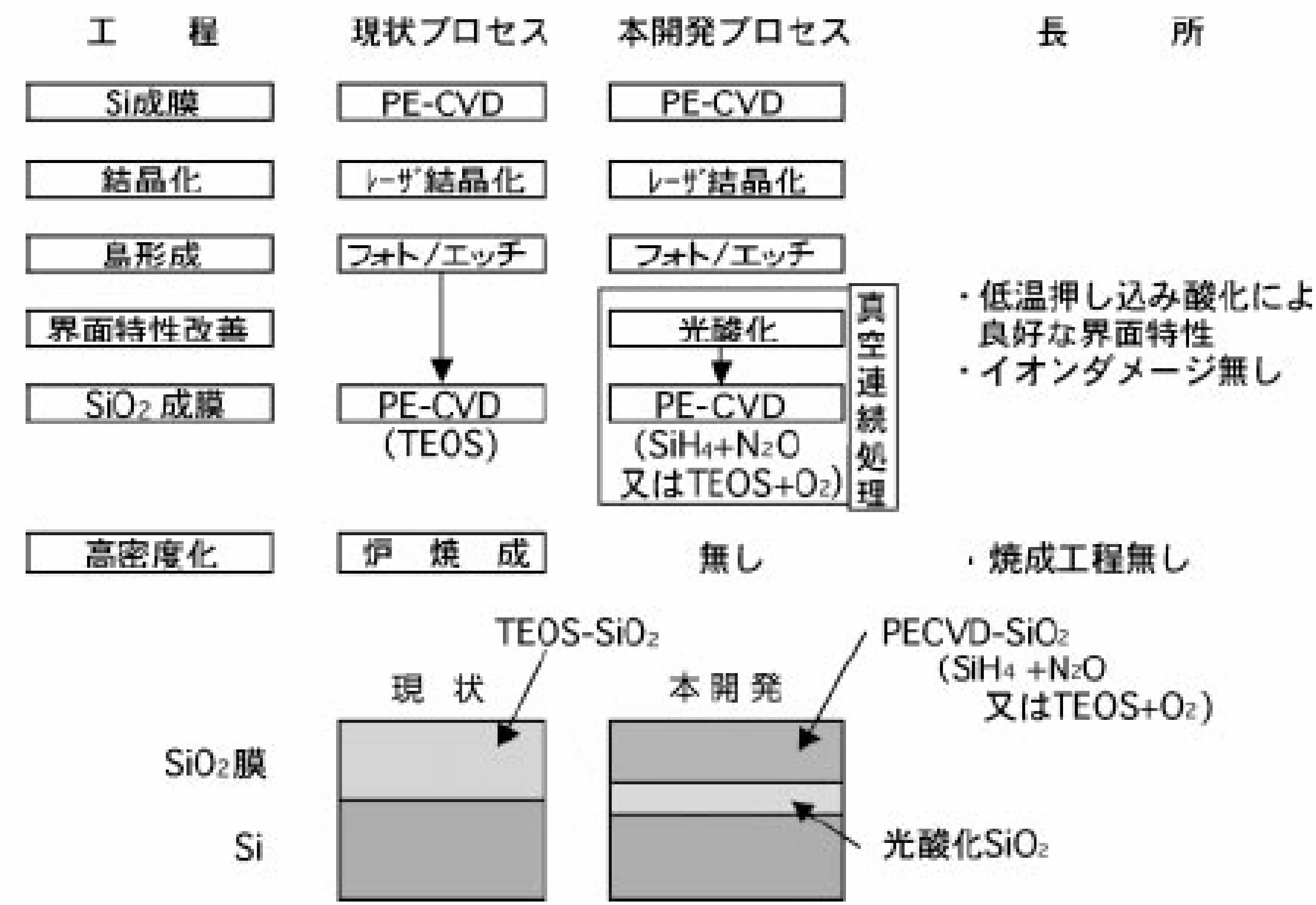



図1　現状と本方法のゲート絶縁膜の形成方法

Fig. 1　Current process and proposed process of gate insulator formation.

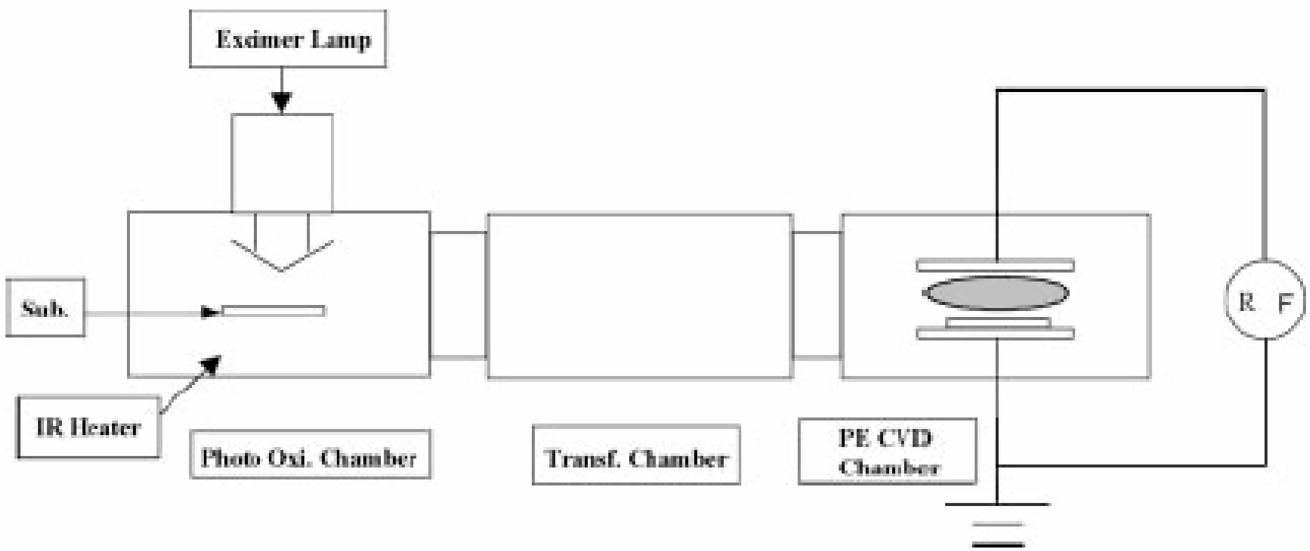



図２　光酸化／PECVD 装置

Fig. 2　Equipment for photo oxidization and PECVD combination process.

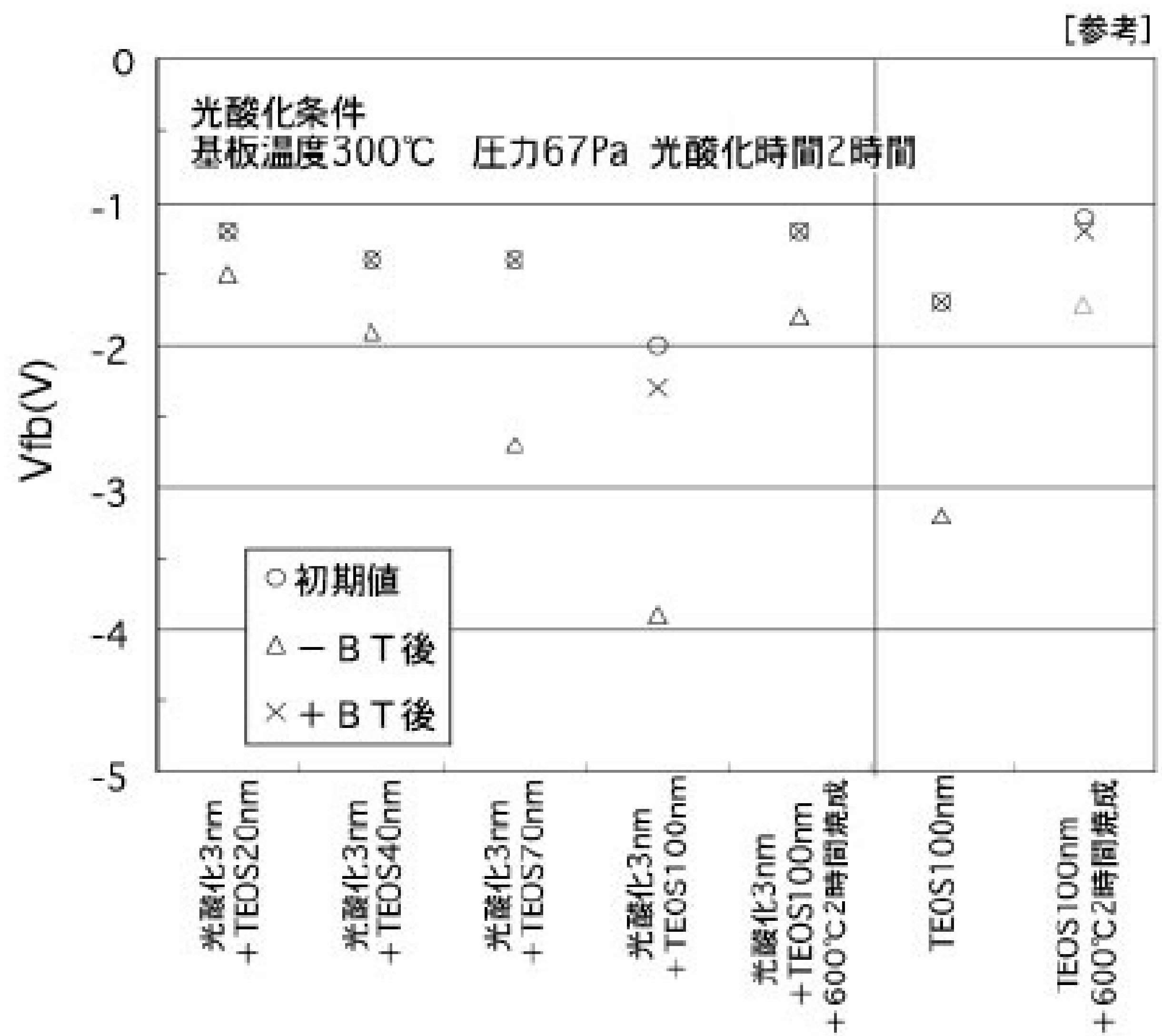



図８　光酸化とPECVD（TEOS+$O_2$）積層絶縁膜のフラットバンド電圧（Vfb）

Fig. 8　Flat band voltage of photo oxide + PECVD ($TEOS+O_2$) stacked insulator.

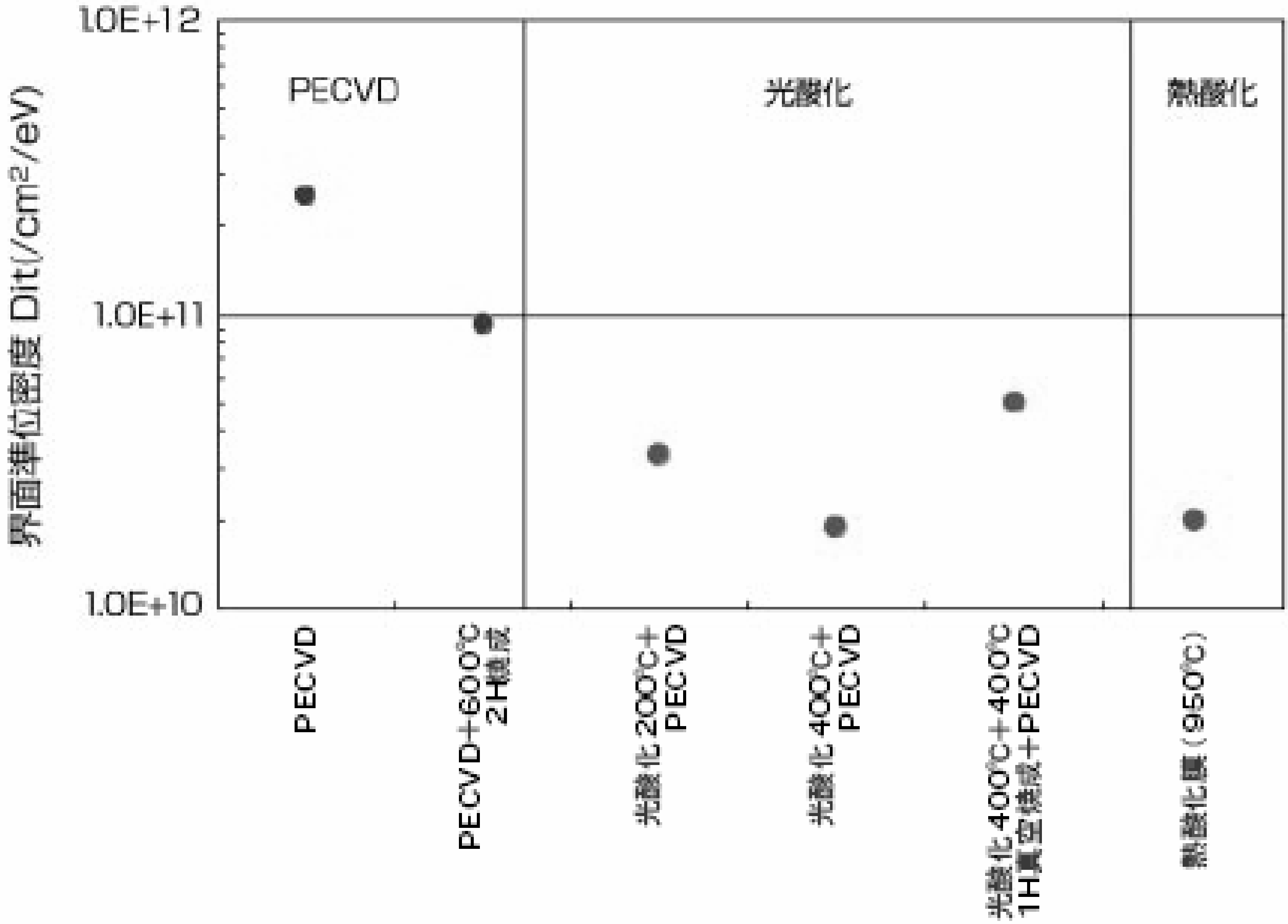



図７　光酸化＋PECVD（$SiH_4$+$N_2O$）積層絶縁膜の界面準位密度

Fig. 7　Interface state density of photo oxide + PECVD ($SiH_4$+$N_2O$) stacked insulator.

# 對各位同學的期許

Boys be ambitious!

Be ambitious not for money or for selfish aggrandizement

財富　地位、聲望、功績

not for that evanescent thing which men call fame.

轉瞬即逝的　名聲

Be ambitious for the attainment of all that a man ought to be.

成就

Clark, William Smith

中國讀書人心態:

「十年寒窗無人問，一舉成名天下知。」

→ 中國讀書人扭曲的心態

重點是要對社會有所貢獻, 而非學歷或官位

「書中自有黃金屋、書中自有顏如玉、書中自有千鍾粟」

創新才有黃金屋及千鐘粟

--- ex. Bill Gates, Nakamura Syuji, TSMC, Jay…etc.

--- evanescent thing which men call fame

不要倚賴“名牌”而要培養實質內涵

LV　BMW　碩博士文憑　IEEE fellow

培養價值判斷能力

沒有先入為主的情形下,
是否知道LV, BMW, 鼎泰豐的價值?

你是幾流?

# 本實驗室介紹: 薄膜元件實驗室 2003年建立

## 宗旨

1. 創新

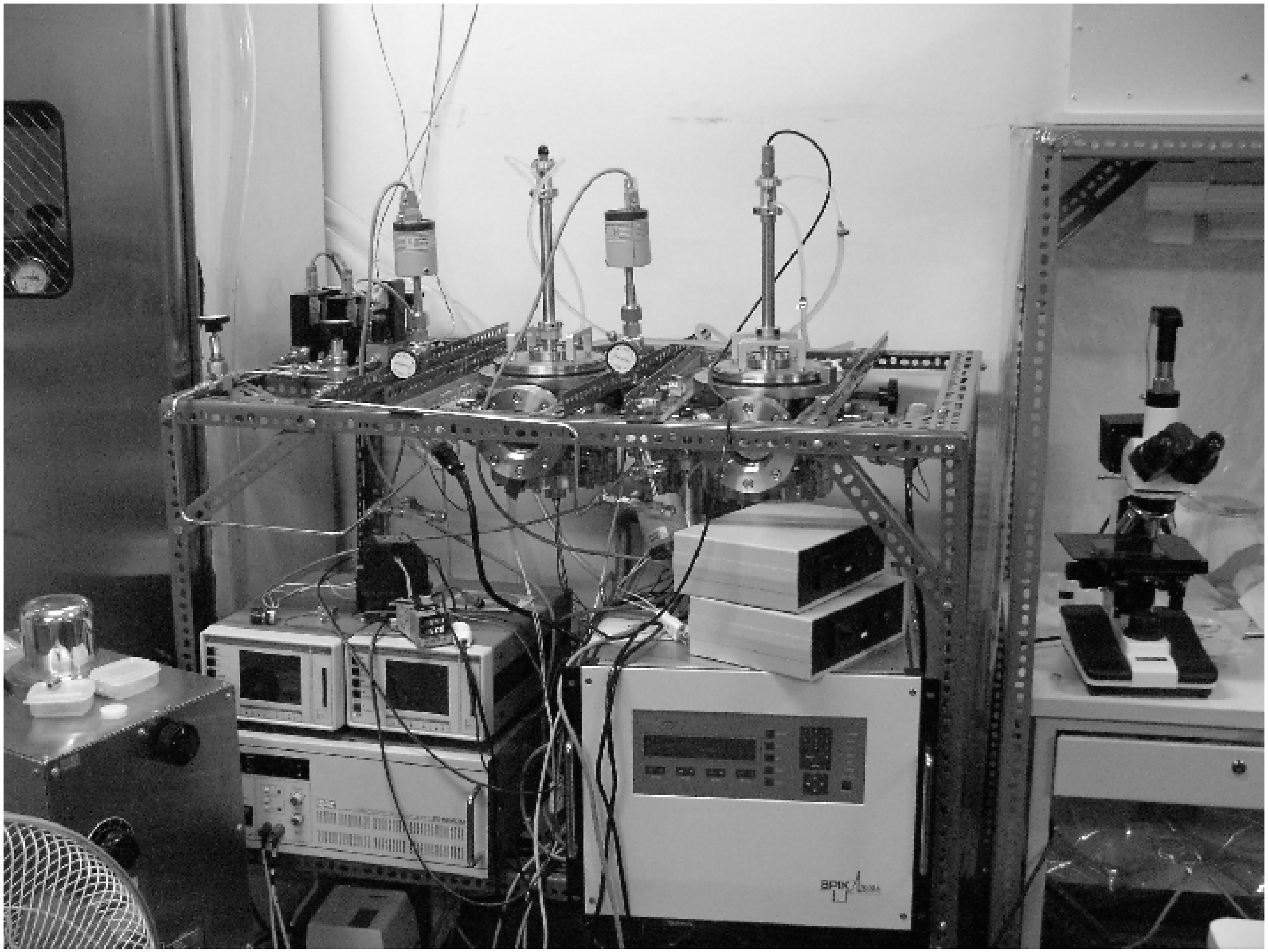
2. 機台創造, 製程創造
   - 低成本, 確保品質, 製程應變力強, 維修迅速

3. 不設無塵室
   - 提供舒適而高效率的研發環境, 亦省下維持費

# 超高濃度臭氧水晶圓洗淨

4台高真空濺鍍機  RF-DC 3 inch

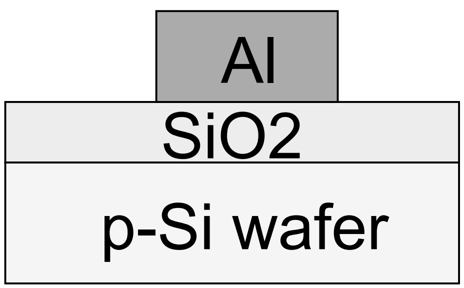
到達真空度  5 x $10^{-7}$ Torr



## 全世界最小蒸鍍機 *(Plug & play ~~)*

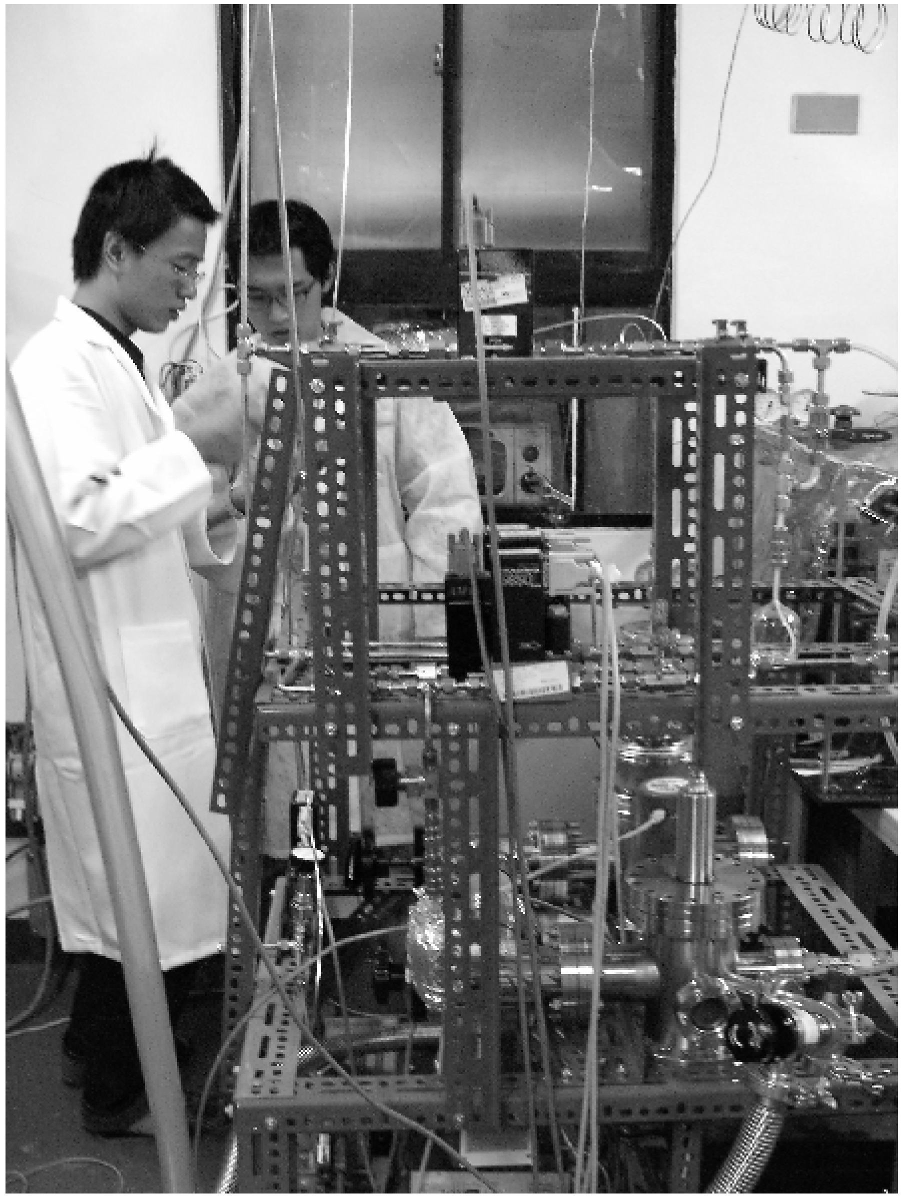
高真空高純度鋁蒸鍍機
1h內到達9*$10^{-7}$Torr,
終極壓力 3*$10^{-8}$Torr

MOS capacitor

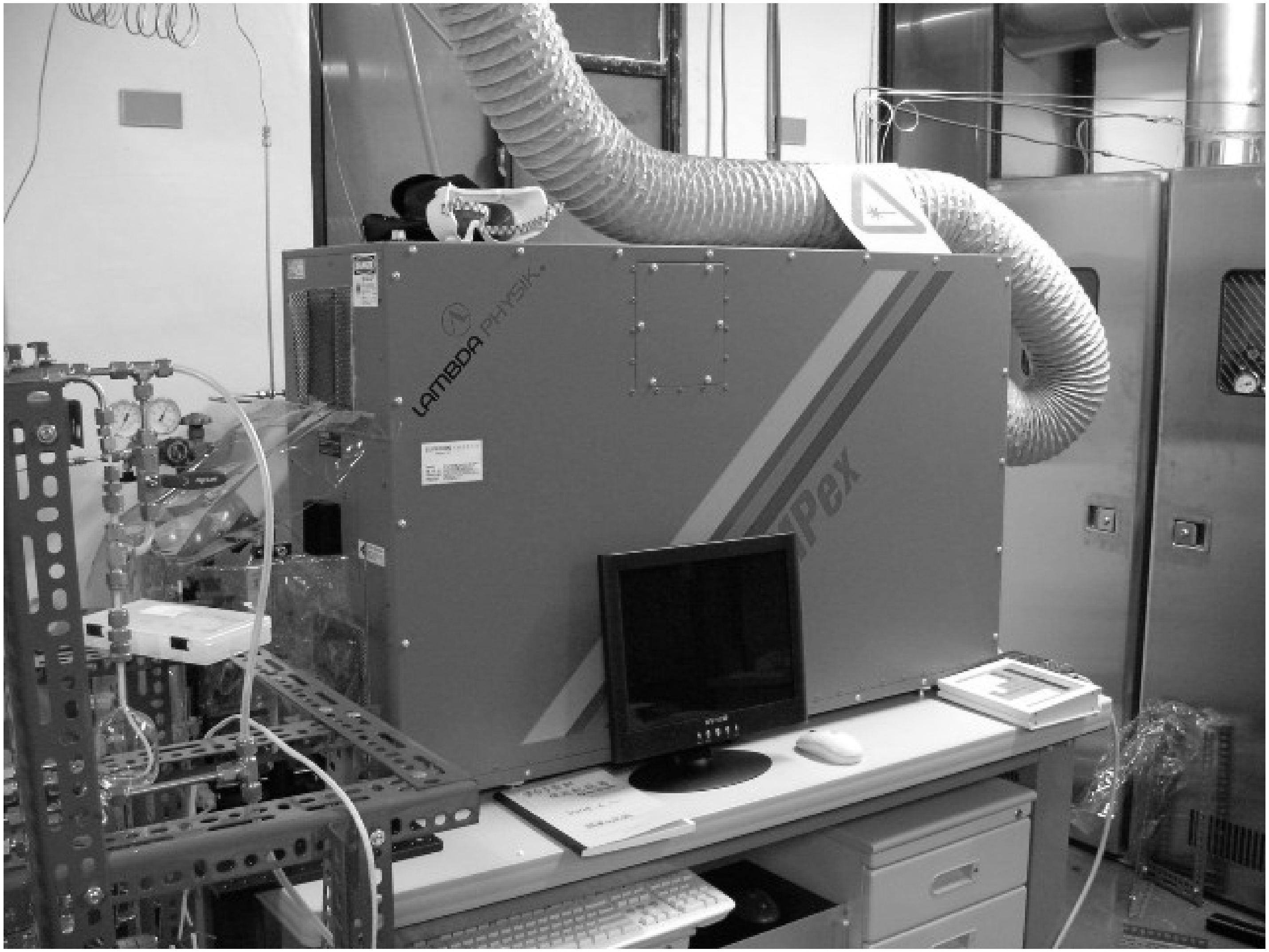



滿足高純度鋁之需求

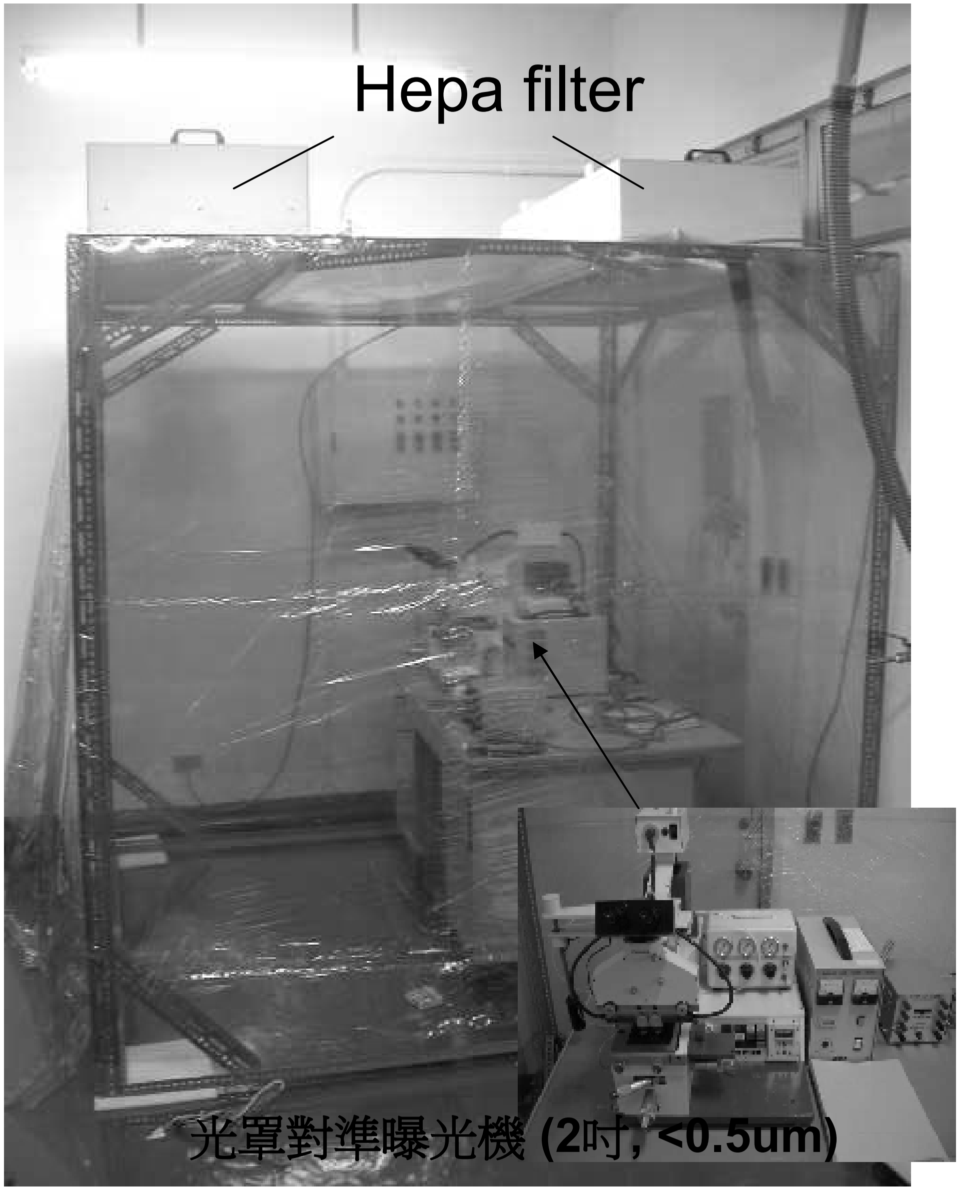
# TEOS PECVD & Hot wire hydrogenator



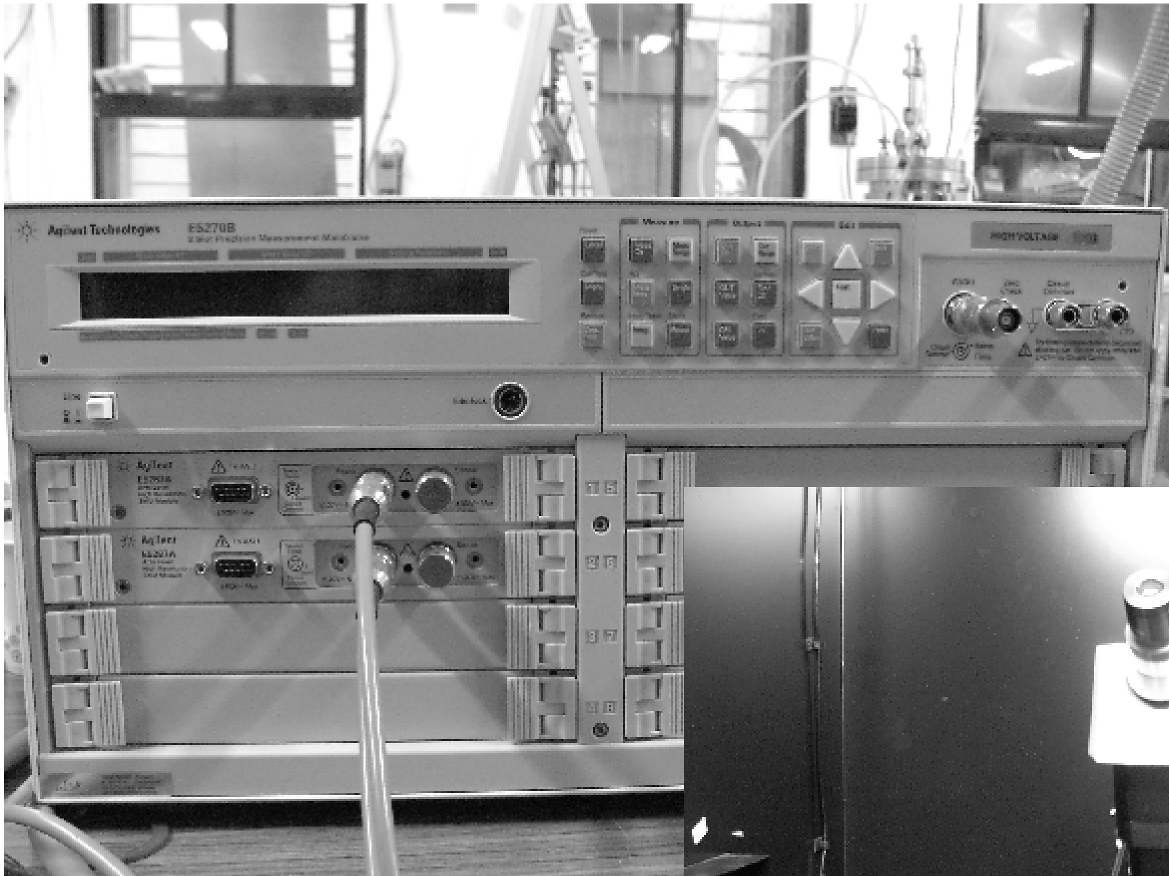
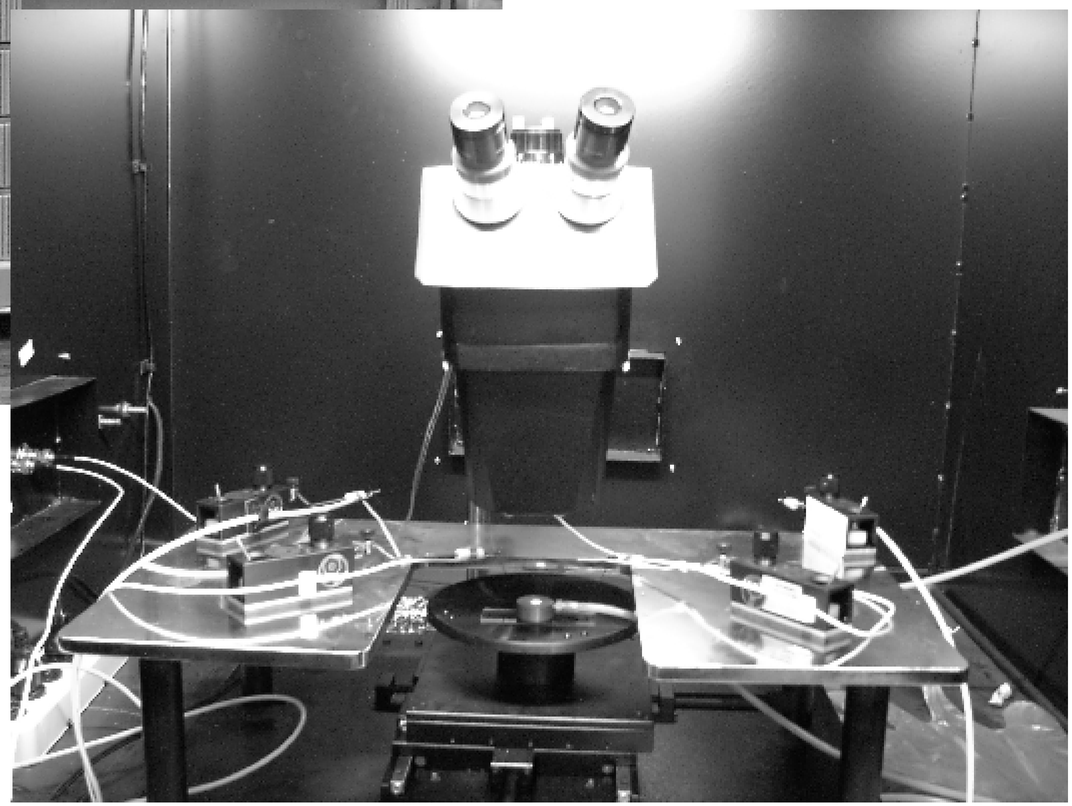
# Excimer laser annealing system



無塵黃光室　　潔淨度<1000?




RTA, Max = $500^{o}C$


Agilent Technologies
E5270B
HIGH VOLTAGE


謝謝聽講!!

歡迎各位前來台科本實驗室攻讀博士學位